

EA30_BM

Schematics Document

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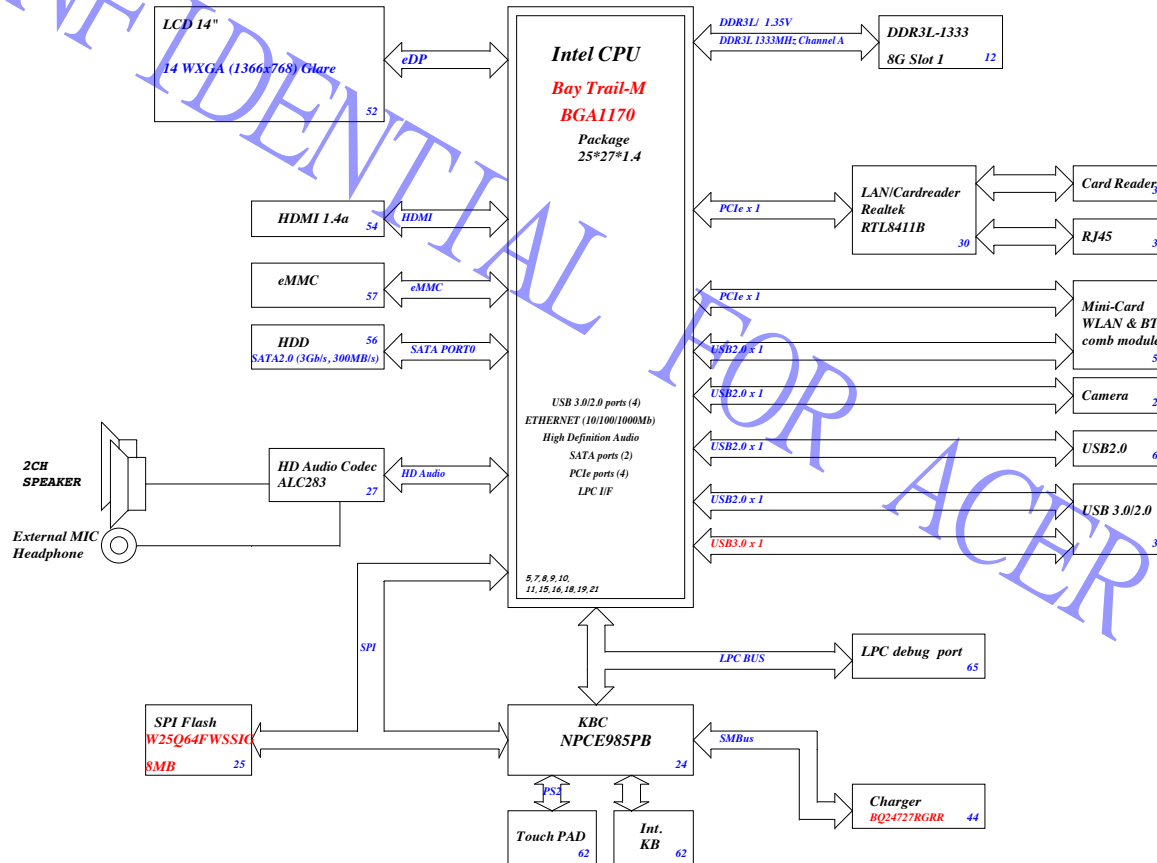
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Title			
Cover Page			
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EA30_BM Board Block Diagram

Project code :
PCB P/N : 14221
Revision : SB



CHARGER	
BQ24727	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
5V_S5	3D3V_S5
DCBATOUT	3D3V_S5
CPU DC/DC	
ISL95833	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SY8208	50
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
SYSTEM DC/DC	
SY8208DQNC	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM LDO	
TLV70218	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
TLV70012	51
INPUTS	OUTPUTS
3D3V_S5	1D2V_S5
Step Down Regulator	
SYW232	51
INPUTS	OUTPUTS
1D0V_S0_P6	1D05V_S0
GPU Core	
RT8812	82
INPUTS	OUTPUTS
DCBATOUT	V6A_CORE
LOAD SWITCH	
TPS22966	37
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
LOAD SWITCH	
TPS22965	37
INPUTS	OUTPUTS
1D0V_S5	1D0V_S0
SYSTEM DC/DC	
SY8208	83
INPUTS	OUTPUTS
DCBATOUT	1D5V_V6A_S0
LOAD SWITCH	
TPS22966	83
INPUTS	OUTPUTS
1D05V_S0	1D5V_V6A_S1
3D3V_S0	3D3V_V6A_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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SSID = CPU

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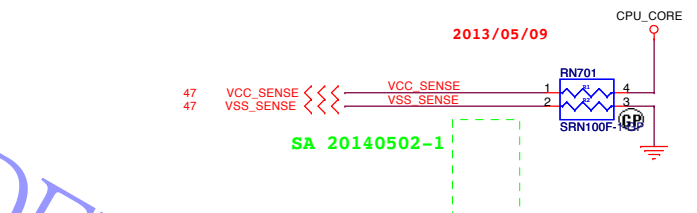
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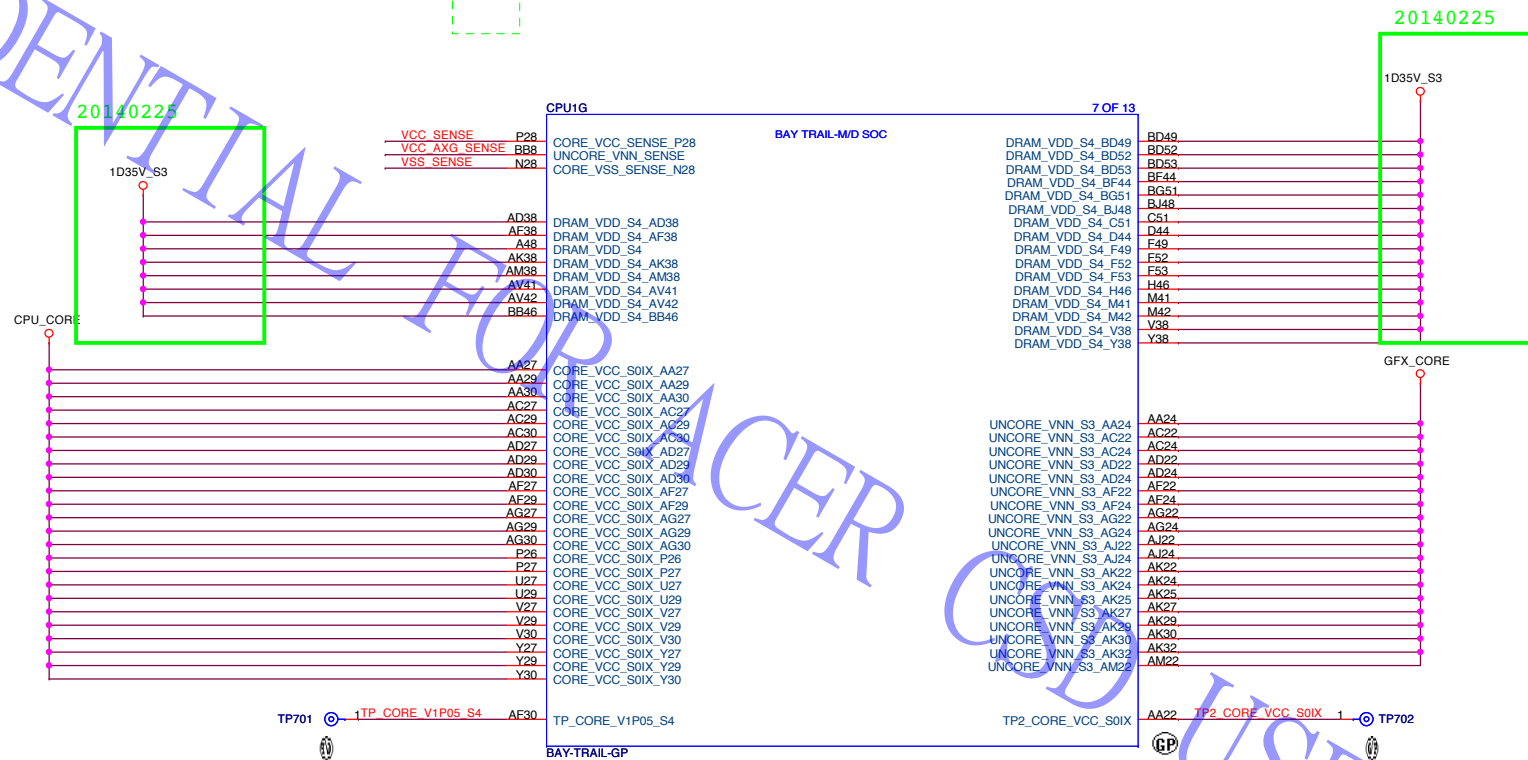
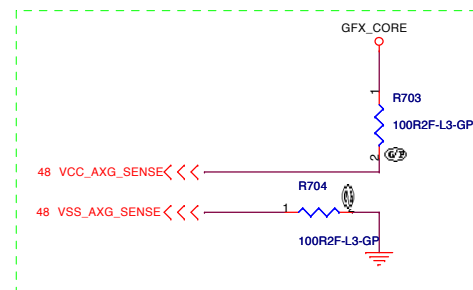
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SSID = CPU



SA 20140502-1



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Title		
CPU (VCC CORE)		
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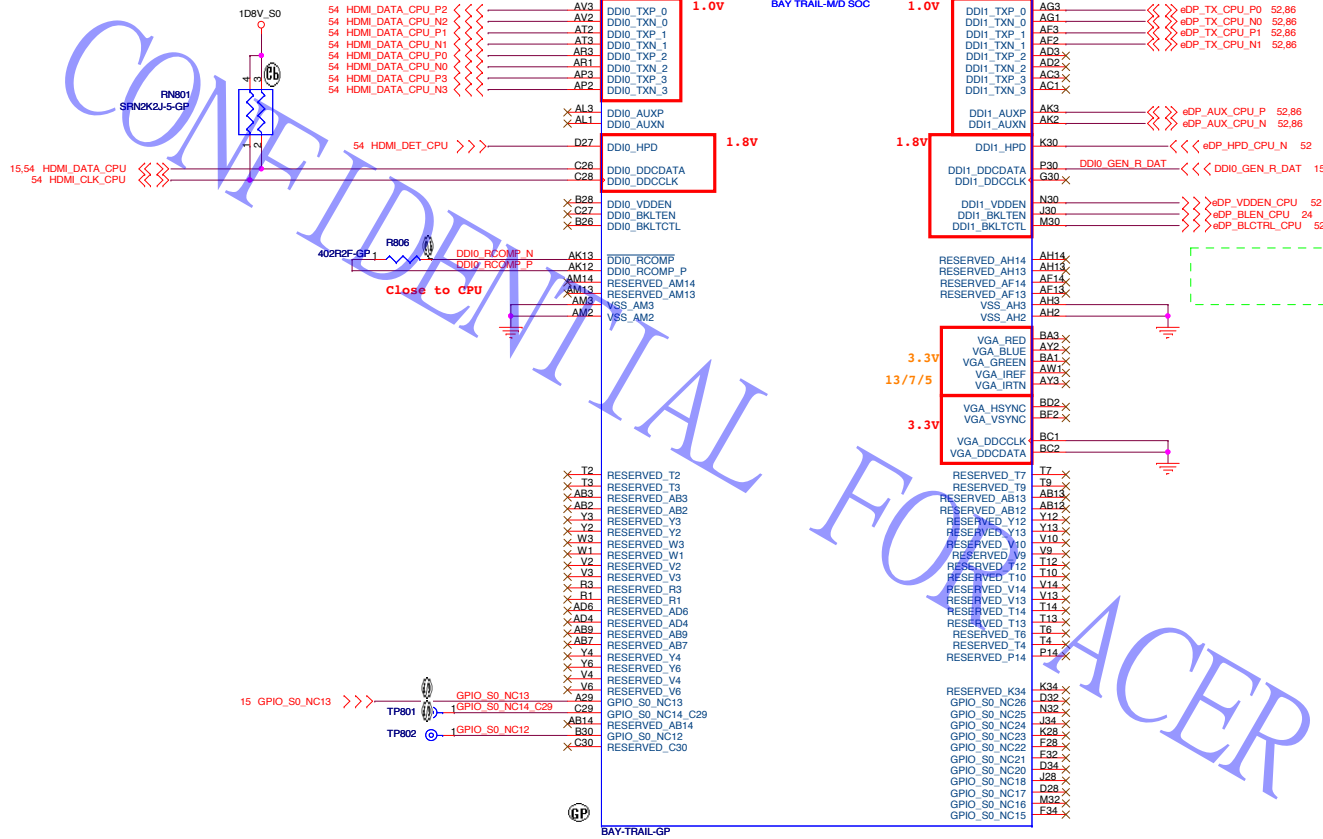
SSID = CPU

HDMI

CPU1C

3 OF 13

PANEL



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Title			
CPU (DD/EDP/GPIO)			
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SSID = CPU

CPU1I 9 OF 13		
BAY TRAIL-M/D SOC		
A11	VSS1	VSS36
A15	VSS2	VSS37
A19	VSS3	VSS38
A23	VSS4	VSS39
A27	VSS5	VSS40
A31	VSS6	VSS41
A35	VSS7	VSS42
A39	VSS8	VSS43
A43	VSS9	VSS44
A47	VSS10	VSS45
AA1	VSS11	VSS46
AA16	VSS12	VSS47
AA19	VSS13	VSS48
AA21	VSS14	VSS49
AA3	VSS15	VSS50
AA32	VSS16	VSS51
AA35	VSS17	VSS52
AA39	VSS18	VSS53
AA53	VSS19	VSS54
AB10	VSS20	VSS55
AB4	VSS21	VSS56
AB41	VSS22	VSS57
AB45	VSS23	VSS58
AB47	VSS24	VSS59
AB48	VSS25	VSS60
AB50	VSS26	VSS61
AB51	VSS27	VSS62
AB6	VSS28	VSS63
AC16	VSS29	VSS64
AC18	VSS30	VSS65
AC19	VSS31	VSS66
AC21	VSS32	VSS67
AC25	VSS33	VSS68
AC33	VSS34	VSS69
AC35	VSS35	VSS70
BAY-TRAIL-GP		

CPU1J 10 OF 13		
BAY TRAIL-M/D SOC		
AG38	VSS71	VSS106
AH4	VSS72	VSS107
AH41	VSS73	VSS108
AH45	VSS74	VSS109
AH7	VSS75	VSS110
AH9	VSS76	VSS111
AJ1	VSS77	VSS112
AJ16	VSS78	VSS113
AJ21	VSS79	VSS114
AJ25	VSS80	VSS115
AJ27	VSS81	VSS116
AJ29	VSS82	VSS117
AJ3	VSS83	VSS118
AJ30	VSS84	VSS119
AJ32	VSS85	VSS120
AJ33	VSS86	VSS121
AJ35	VSS87	VSS122
AJ38	VSS88	VSS123
AJ53	VSS89	VSS124
AK10	VSS90	VSS125
AK14	VSS91	VSS126
AK16	VSS92	VSS127
AK33	VSS93	VSS128
AK41	VSS94	VSS129
AK44	VSS95	VSS130
AM12	VSS96	VSS131
AM19	VSS97	VSS132
AM24	VSS98	VSS133
AM25	VSS99	VSS134
AM29	VSS100	VSS135
AM33	VSS101	VSS136
AM35	VSS102	VSS137
AM36	VSS103	VSS138
AM40	VSS104	VSS139
M28	VSS105	VSS140
BAY-TRAIL-GP		

CPU1K 11 OF 13		
BAY TRAIL-M/D SOC		
AT24	VSS141	VSS176
AT27	VSS142	VSS177
AT30	VSS143	VSS178
AT35	VSS144	VSS179
AT38	VSS145	VSS180
AT4	VSS146	VSS181
AT47	VSS147	VSS182
AT52	VSS148	VSS183
AU1	VSS149	VSS184
AU24	VSS150	VSS185
AU3	VSS151	VSS186
AU30	VSS152	VSS187
AU38	VSS153	VSS188
AU51	VSS154	VSS189
AV12	VSS155	VSS190
AV13	VSS156	VSS191
AV14	VSS157	VSS192
AV18	VSS158	VSS193
AV19	VSS159	VSS194
AV24	VSS160	VSS195
AV27	VSS161	VSS196
AV30	VSS162	VSS197
AV35	VSS163	VSS198
AV38	VSS164	VSS199
AV47	VSS165	VSS200
AV51	VSS166	VSS201
AV7	VSS167	VSS202
AW13	VSS168	VSS203
AW19	VSS169	VSS204
AW27	VSS170	VSS205
AW3	VSS171	VSS206
AW35	VSS172	VSS207
AY10	VSS173	VSS208
AY22	VSS174	VSS209
AY32	VSS175	VSS210
BAY-TRAIL-GP		

CPU1L 12 OF 13		
BAY TRAIL-M/D SOC		
BF30	VSS211	VSS246
BF36	VSS212	VSS247
BF4	VSS213	VSS248
BF41	VSS214	VSS249
BG31	VSS215	VSS250
BG34	VSS216	VSS251
BG39	VSS217	VSS252
BG42	VSS218	VSS253
BG45	VSS219	VSS254
BG49	VSS220	VSS255
BJ11	VSS221	VSS256
BJ15	VSS222	VSS257
BJ19	VSS223	VSS258
BJ23	VSS224	VSS259
BJ27	VSS225	VSS260
BJ31	VSS226	VSS261
BJ35	VSS227	VSS262
BJ39	VSS228	VSS263
BJ43	VSS229	VSS264
BJ47	VSS230	VSS265
BJ7	VSS231	VSS266
C14	VSS232	VSS267
C31	VSS233	VSS268
C34	VSS234	VSS269
C39	VSS235	VSS270
C42	VSS236	VSS271
C45	VSS237	VSS272
C49	VSS238	VSS273
D12	VSS239	VSS274
D16	VSS240	VSS275
D24	VSS241	VSS276
D30	VSS242	VSS277
D36	VSS243	VSS278
D38	VSS244	VSS279
E19	VSS245	VSS280
E35		
BAY-TRAIL-GP		

CPU1M 13 OF 13		
BAY TRAIL-M/D SOC		
K9	VSS281	VSS316
L13	VSS282	VSS317
L19	VSS283	VSS318
L35	VSS284	VSS319
M19	VSS285	VSS320
M26	VSS286	VSS321
M27	VSS287	VSS322
M34	VSS288	VSS323
M35	VSS289	VSS324
M38	VSS290	VSS325
M47	VSS291	VSS326
M51	VSS292	VSS327
N1	VSS293	VSS328
N16	VSS294	VSS329
N38	VSS295	VSS330
N51	VSS296	VSS331
P13	VSS297	VSS332
P19	VSS298	VSS333
P20	VSS299	VSS334
P24	VSS300	VSS335
P32	VSS301	VSS336
P35	VSS302	VSS337
P39	VSS303	VSS338
P4	VSS304	VSS339
P47	VSS305	VSS340
P52	VSS306	VSS341
P9	VSS307	VSS342
T40	VSS308	VSS343
U1	VSS309	VSS344
U11	VSS310	VSS345
U12	VSS311	VSS346
U14	VSS312	VSS347
U21	VSS313	VSS348
	VSS314	VSS349
	VSS315	VSS350
BAY-TRAIL-GP		

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CPU (VSS)		
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CPU_CORE

CPU_CORE

SA 20140225 change to 0805

C1027

C1023

C1025

C1009

C1010

C1011

C1024

C1012

C1013

SC22U6D3V5MX-L3-GP

SC22U6D3V5MX-L3-GP

SC22U6D3V5MX-L3-GP

SC22U6D3V3MX-1-GP

SC22U6D3V3MX-1-GP

SC22U6D3V3MX-1-GP

SC22U6D3V5MX-L3-GP

SC22U6D3V3MX-1-GP

SC22U6D3V5MX-L3-GP

SA 20140416 change to 0603

Cap Modify
(For power)

SA 20140225 P7 del close gap

1D35V_S3

SA 20140225 P7 del close gap

1D35V_S3

-1M 2040630

C1001

C1002

C1003

C1004

C1005

C1006

C1007

C1008

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

Do Not Stuff

Do Not Stuff

Do Not Stuff

Do Not Stuff

C1014

C1015

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

Close pin AD38 & AF38

Cap Modify

Cap Modify

GFX_CORE

GFX_CORE

SA 20140225 change to 0603

C1016

C1017

C1018

C1019

C1020

C1021

SC22U6D3V3MX-1-GP

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

SC22U6D3V3MX-1-GP

SC22U6D3V3MX-1-GP

SC22U6D3V5MX-L3-GP

Cap Modify
(For power)Cap Modify
(For power)

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Title

CPU (Power CAP1)

Size
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Document Number

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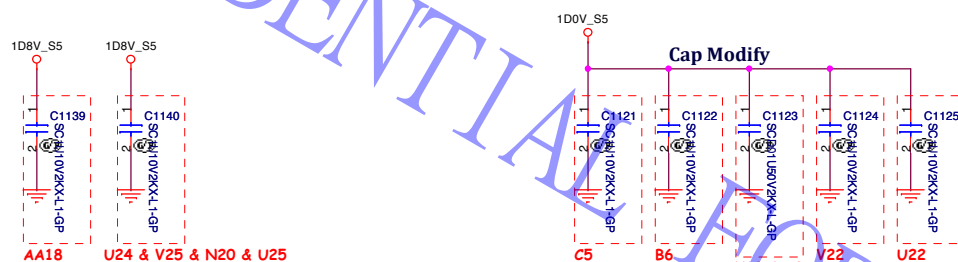
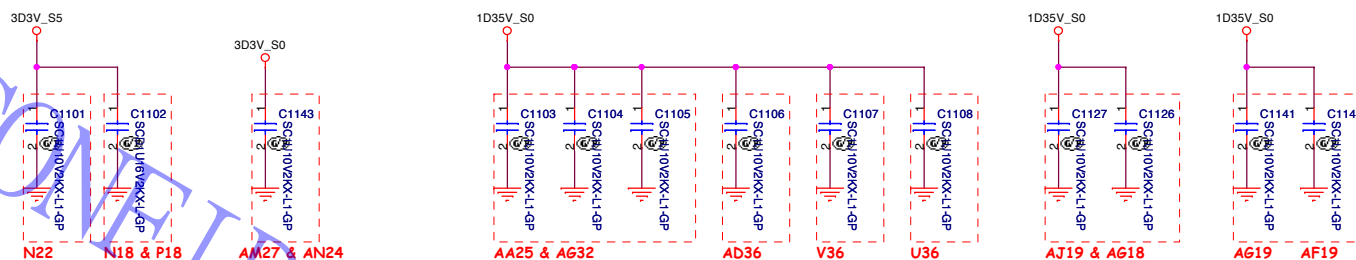
Rev
-1

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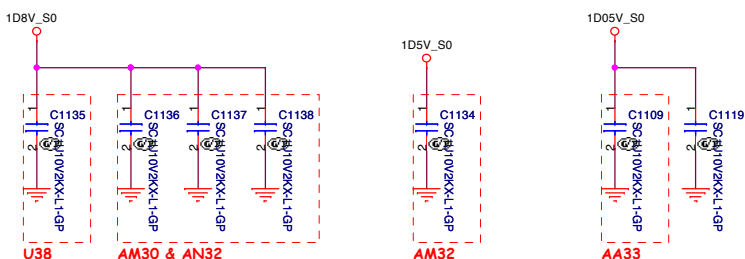
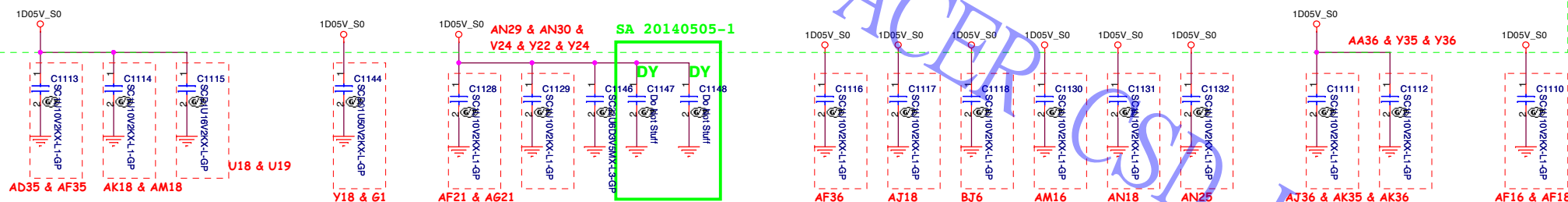
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Cap Modify



SA 20140418

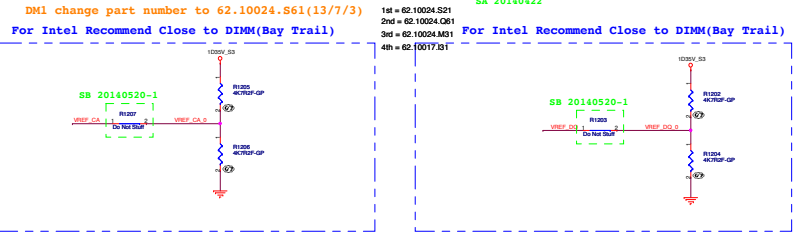
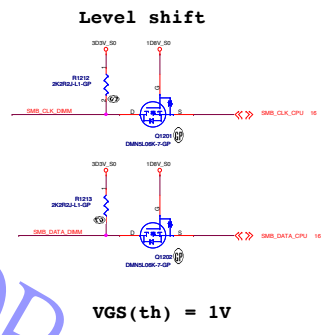
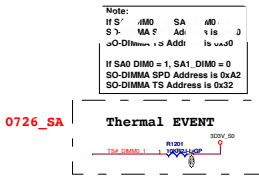
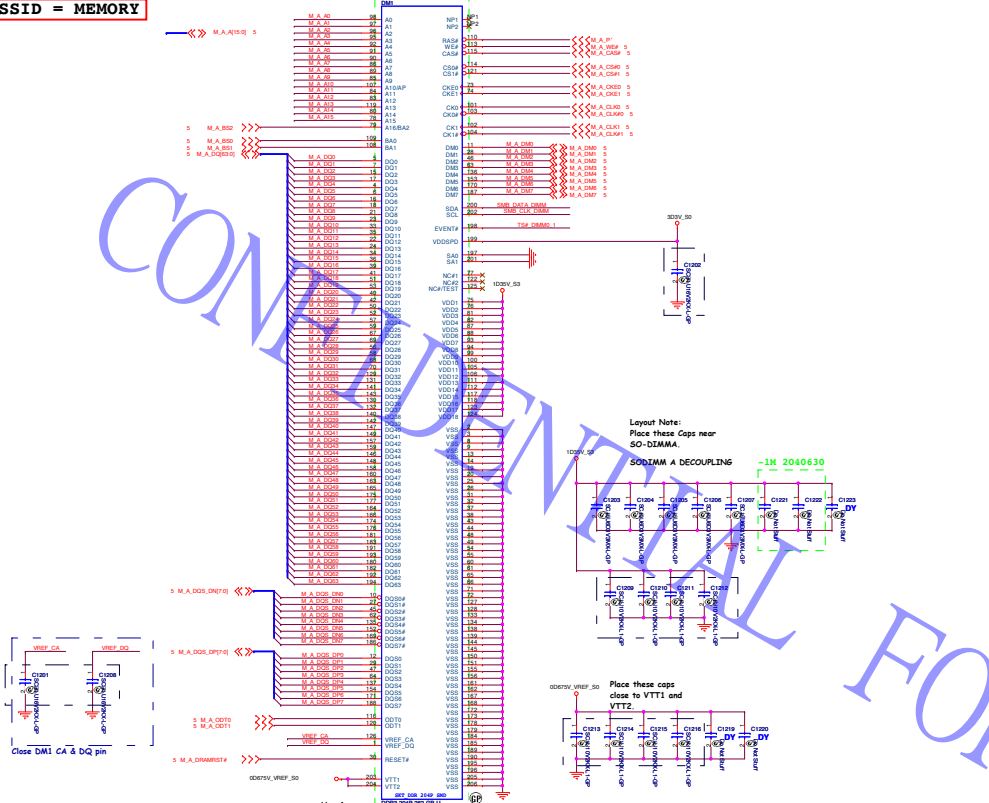


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CPU (Power CAP2)			
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SSID = MEMORY



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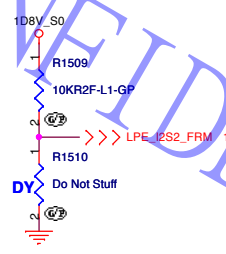
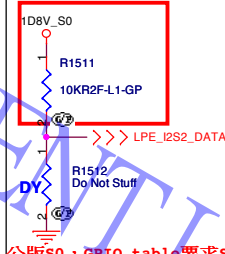
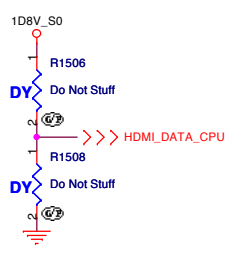
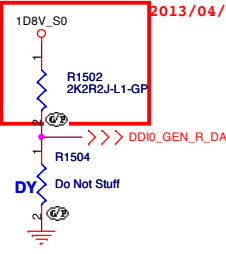
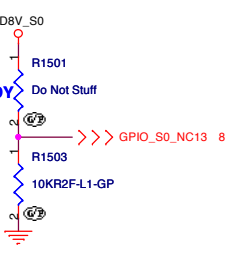
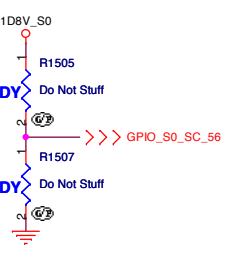
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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED OUTSIDE KOZ AREA
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI1 Detect	DDI0 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI1_DDCDATA	DDI0_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	RN801 PH DDI1 detected	DDI0 detected	DDI1 detected	
Low	LPC	Override	DDI1 not detected	DDI0 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

30.2 LPE_I2S2_DATAOUT / GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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CPU(STRAP)

Size
A3

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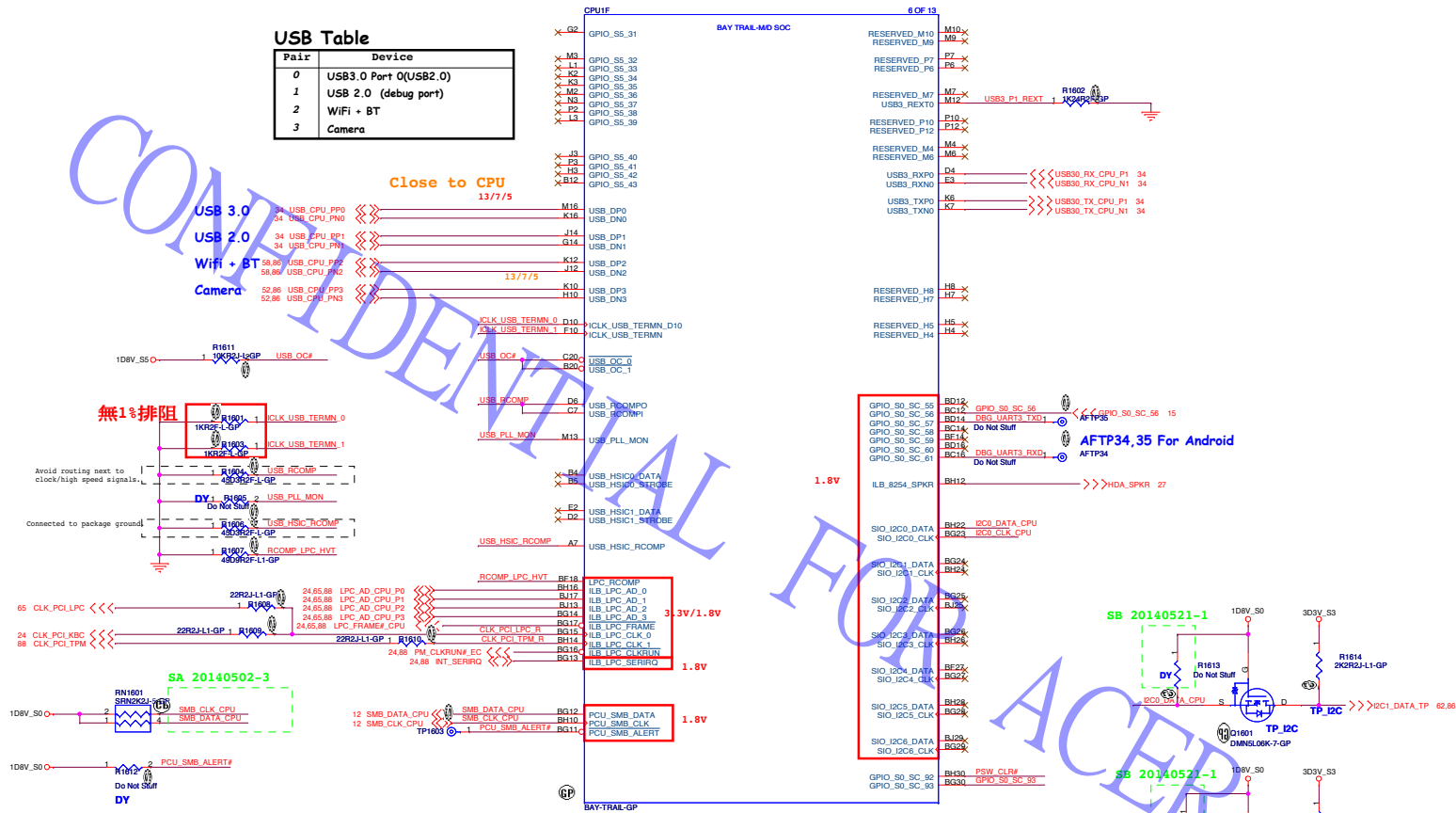
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SSID = PCH

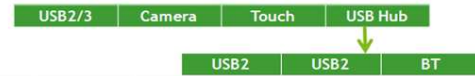
USB Table

Pair	Device
0	USB3.0 Port 0(USB2.0)
1	USB 2.0 (debug port)
2	WiFi + BT
3	Camera

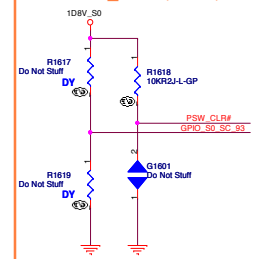


USB Port Routing Guide for Bay Trail-M

WO/ Lighting Bolt(Can support 3 USB I/O Ports)



For PSW_CLR# (5/14)



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CPU (USB/LPC/GPIO)			
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SSID = PCH

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Title

CPU (DMI/FDI/PM)

Size
A4

Document Number

EA30 BM

Rev
-1

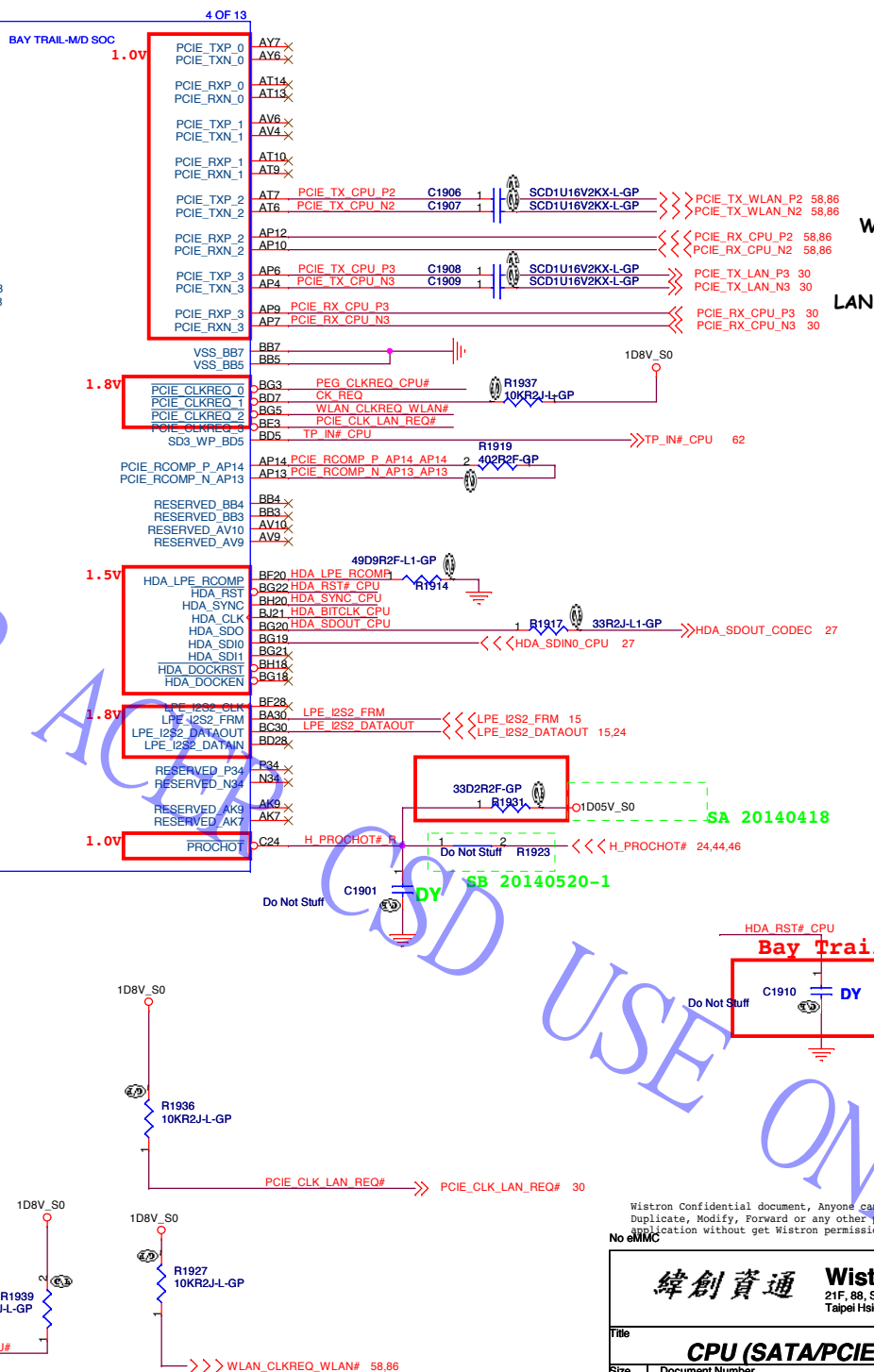
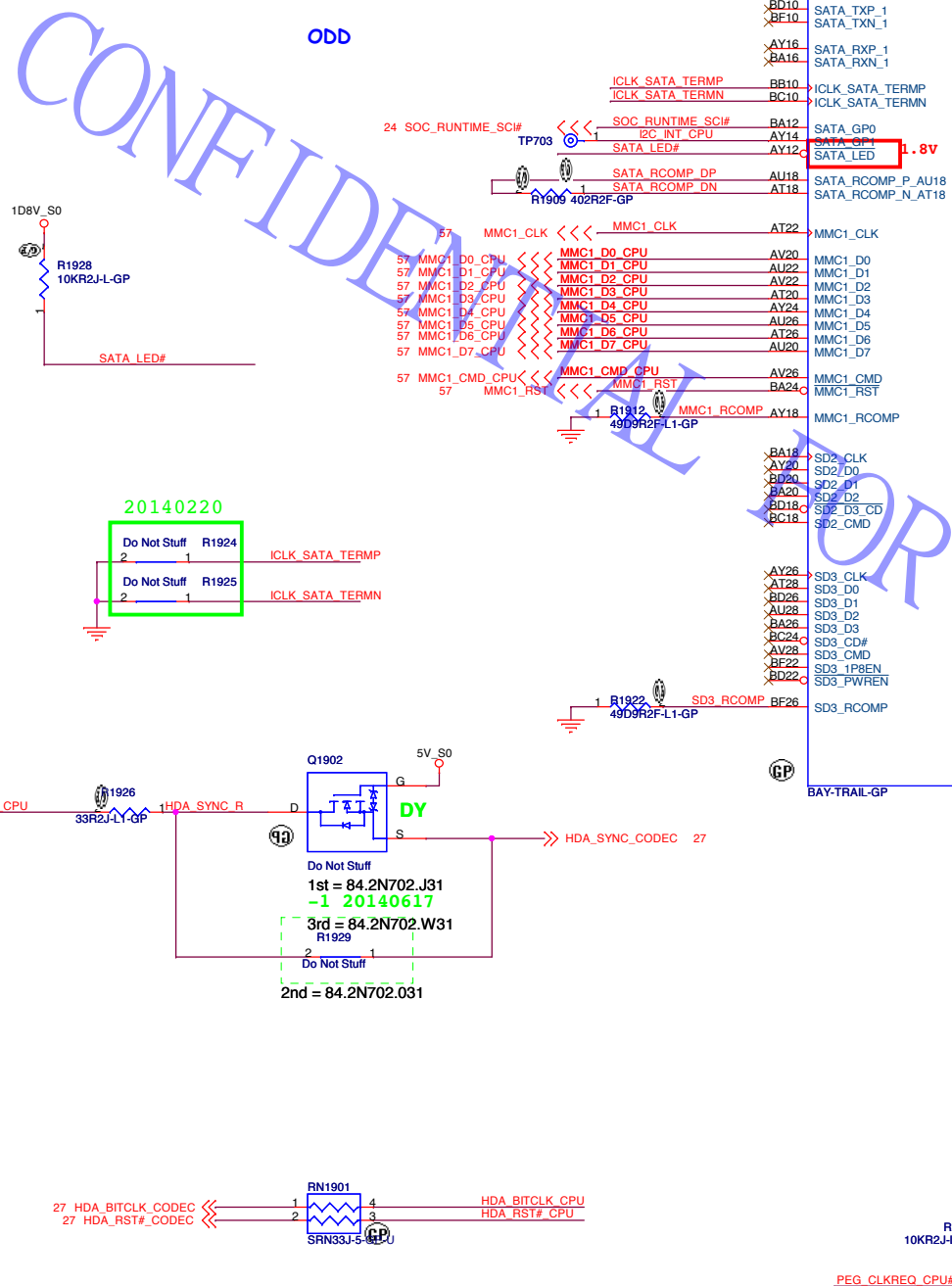
Date: Tuesday, July 08, 2014

Sheet 17 of 102

SSID = PCH

HDD

ODD



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Title			
CPU (SATA/PCIE/IHDA)			
Size A3	Document Number		Rev
	EA30 BM		-1
Date:	Tuesday, July 08, 2014	Sheet	19 of 102

SSID = PCH

Blanking

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Title

Reserved

Size
A4

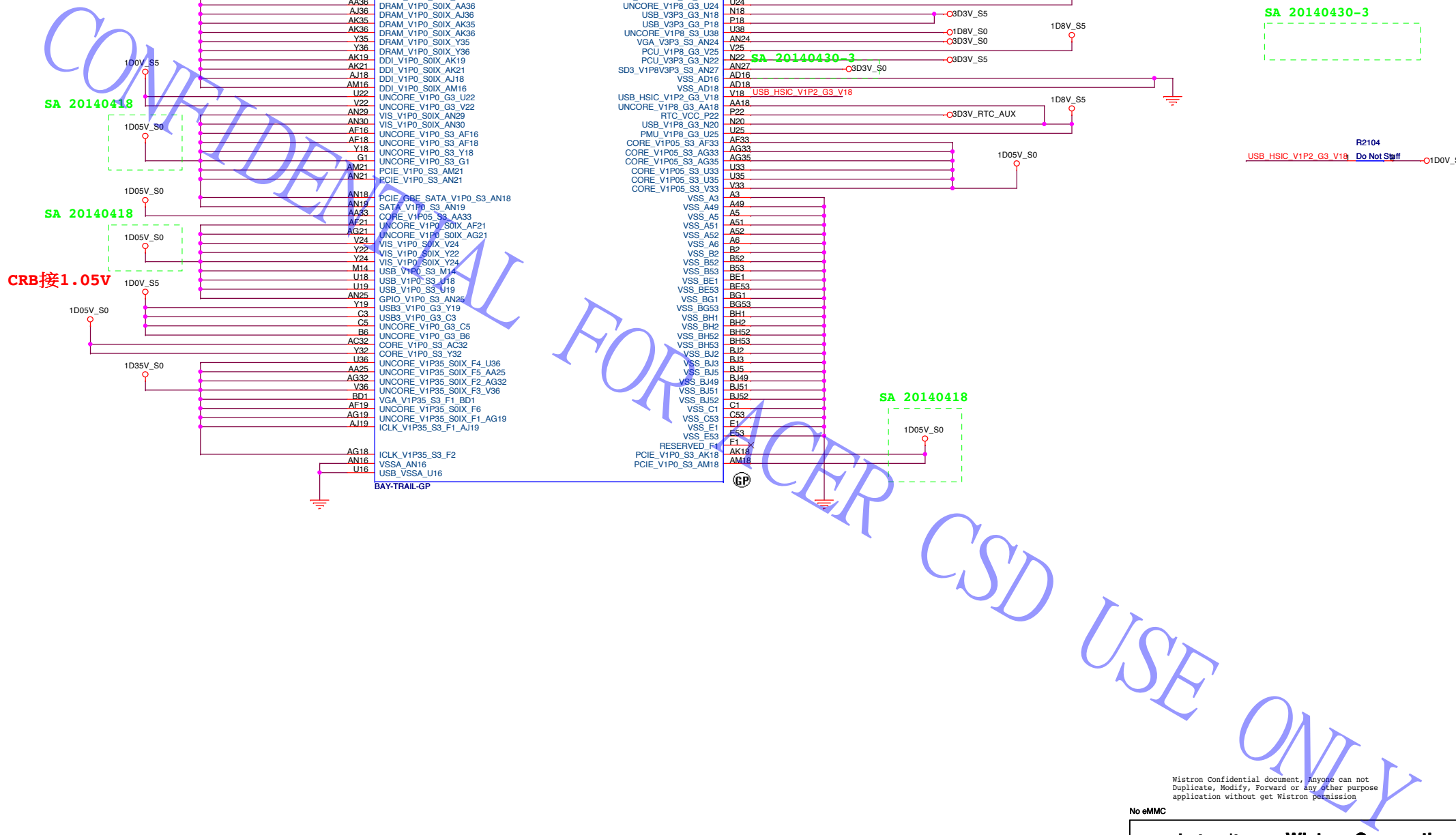
Document Number

EA30 BM

Rev
-1

Date: Tuesday, July 08, 2014

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13/8/22

SA 20140430-3

R2104

USB_HSIC_V1P2_G3_V18 Do Not Stuff 1D0V_S5

SA 20140418

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Title			CPU (POWER1)	
Size	Document Number		Rev	
A3	EA30 BM		-1	
Date:	Tuesday, July 08, 2014		Sheet	21 of 102

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Title			
Reserved			
Size Custom	Document Number EA30 BM		Rev -1
Date: Tuesday, July 08, 2014		Sheet 22 of	102

SSID = PCH

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Title

CPU (VSS)

Size
Custom

Document Number

EA30 BM

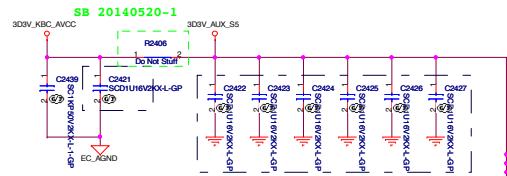
Rev

-1

Date: Tuesday, July 08, 2014

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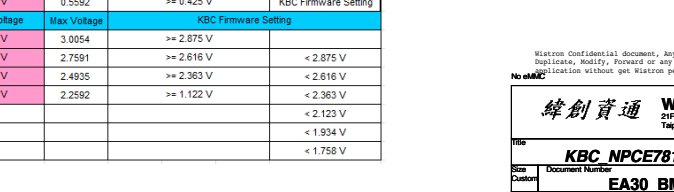
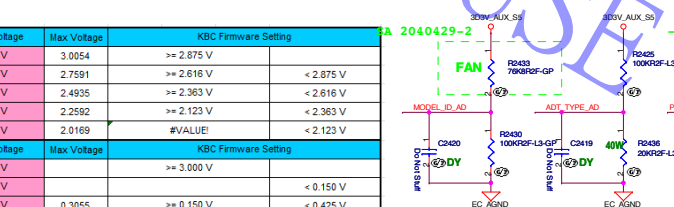
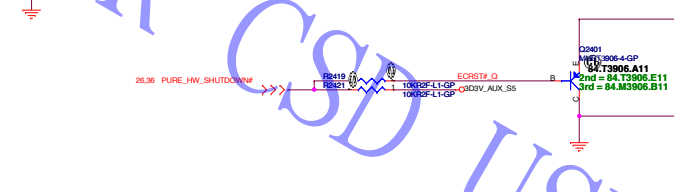
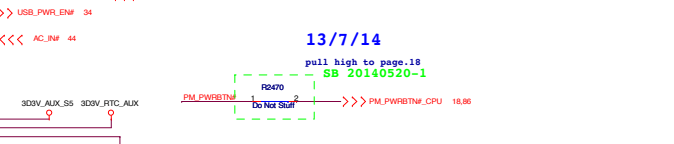
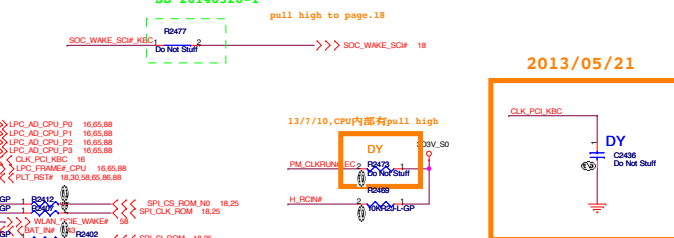
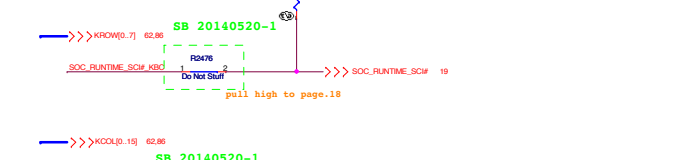
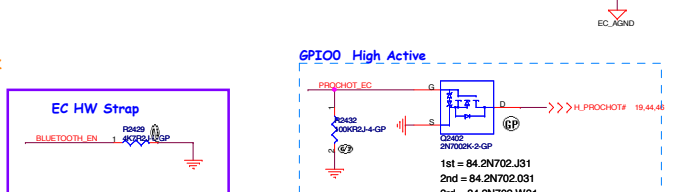
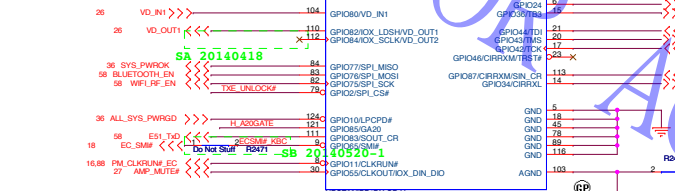
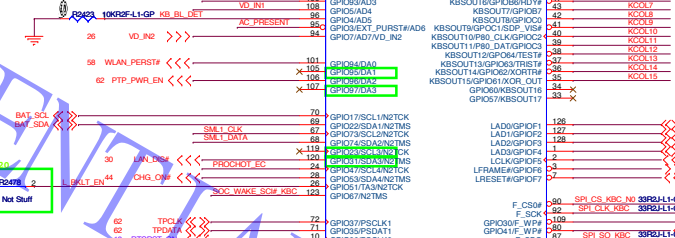
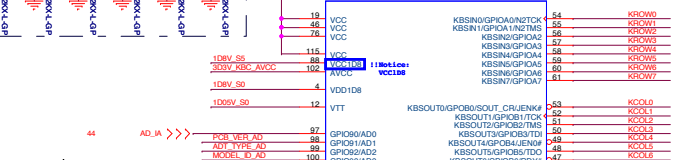
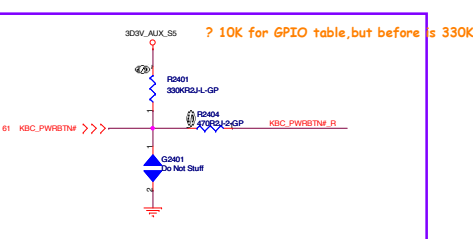
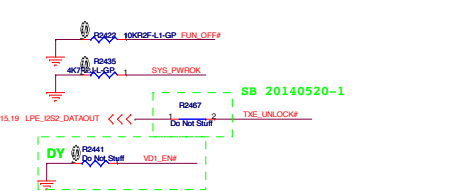
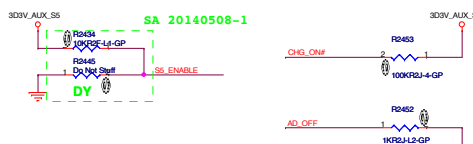
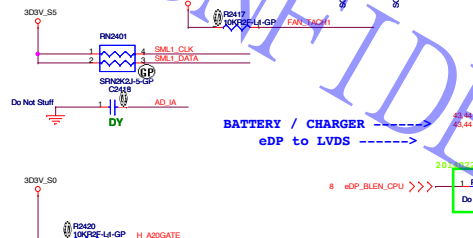
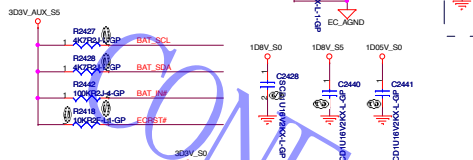
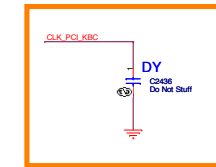
SSID = KBC



Level shift



2013/05/21



PCB_VER_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.0054	3.0054	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	>= 2.618 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.383 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	#VALUE!	< 2.123 V
ADT_TYPE_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V	3.300 V	>= 3.000 V	
90W	100.0 K	N/A	0.000 V	0.000 V		< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	>= 0.150 V	< 0.425 V
40W	20.0 K	100.0 K	0.550 V	0.5592	>= 0.425 V	KBC Firmware Setting
MODEL_ID_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
EA30_FANLESS	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V	
EA30_FAN	100.0 K	20.0 K	2.750 V	2.7591	>= 2.618 V	< 2.875 V
EA53_FANLESS	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
EA53_FAN	100.0 K	47.0 K	2.245 V	2.2592	>= 2.122 V	< 2.383 V
EA30_FANLESS_FAN0	100.0 K	64.9 K			>= 2.123 V	< 2.123 V
EA30_FAN_FAN0	100.0 K	76.8 K			>= 1.934 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K			>= 1.758 V	< 1.758 V

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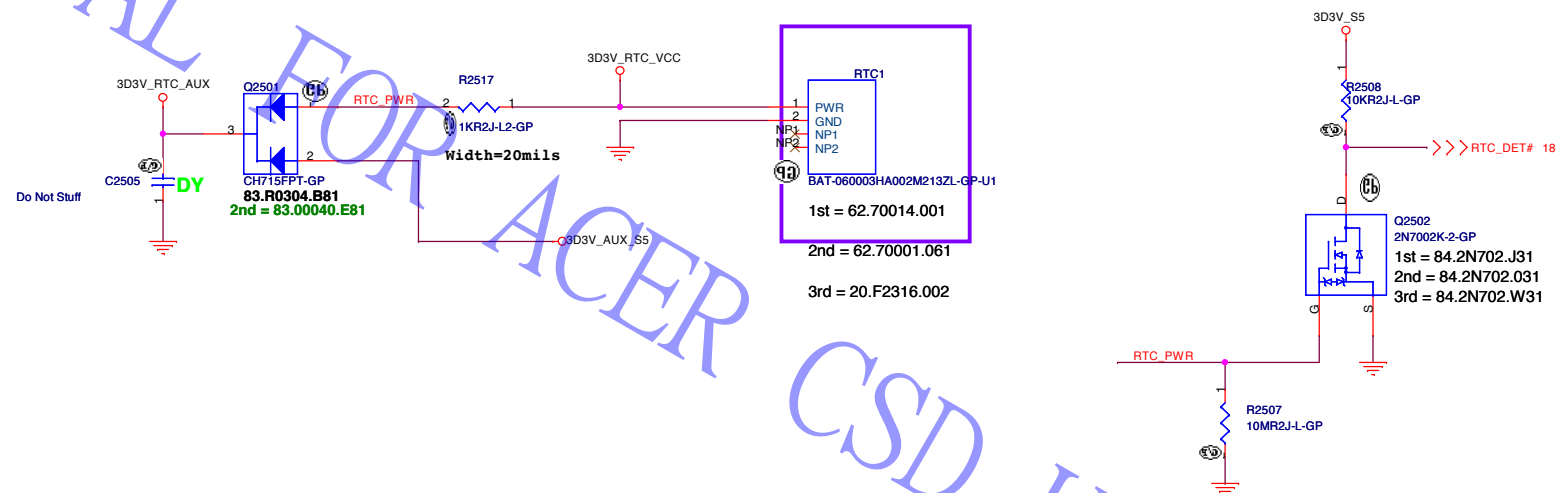
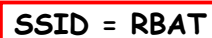
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsein 301, Taiwan, R.O.C.

File No. KBC NPCE781LA

Doc. Number EA30 BM

Date: Tuesday, July 08, 2014 Sheet 24 of 102

SP1 FLASH ROM (8M бYTE) иС PCH



SPI ROM Equal length need to less than 500mil

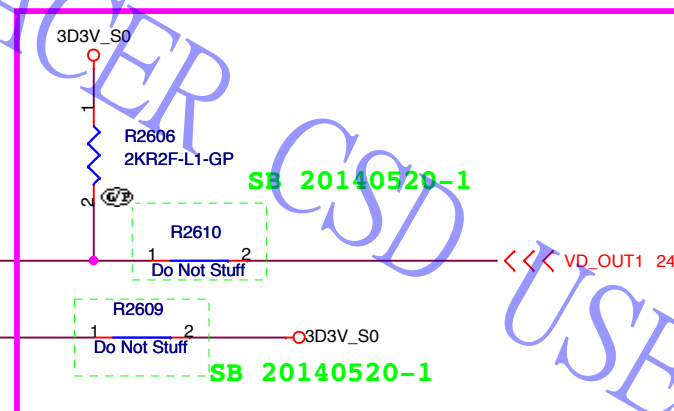
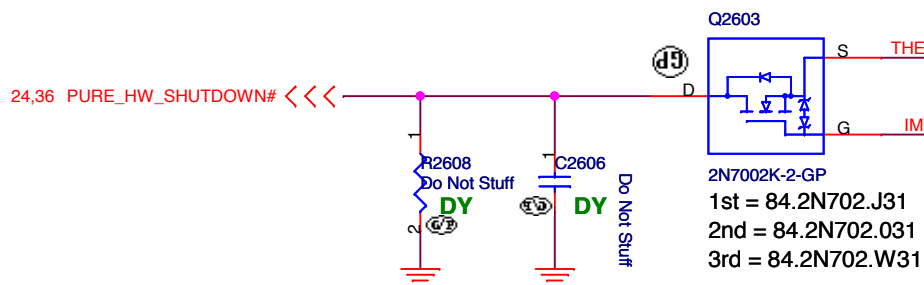
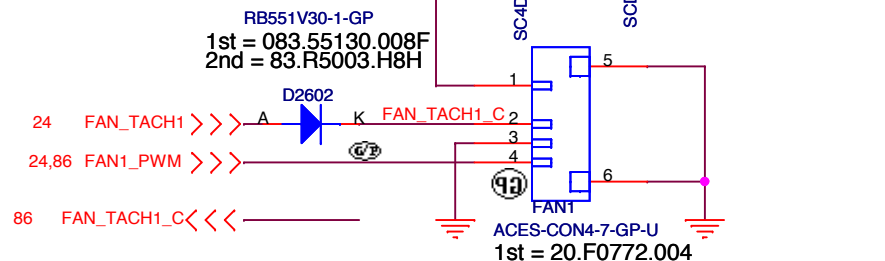
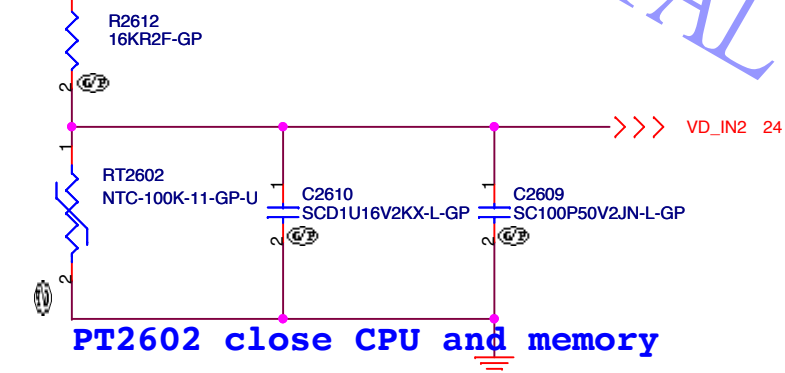
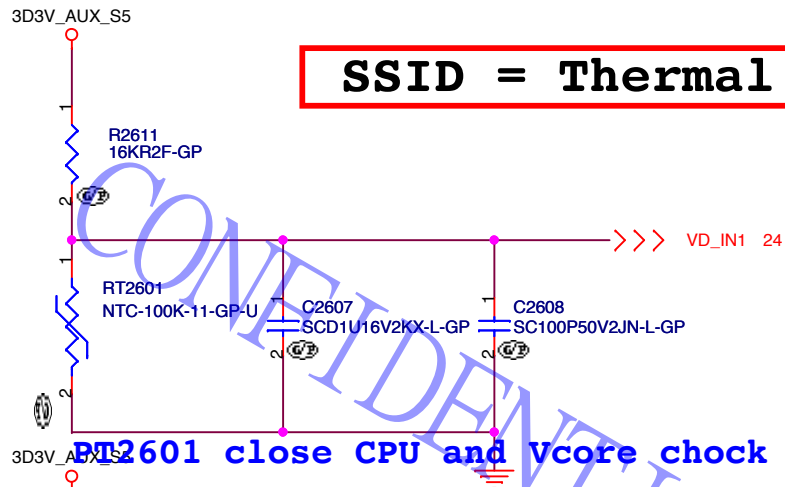
72.25010.N01

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Title			
Flash(KBC+PCH)/RTC			
Size A3	Document Number		Rev
	EA30 BM		-1
Date:	Tuesday, July 08, 2014	Sheet	25 of 102

SSID = Thermal



No eMMC

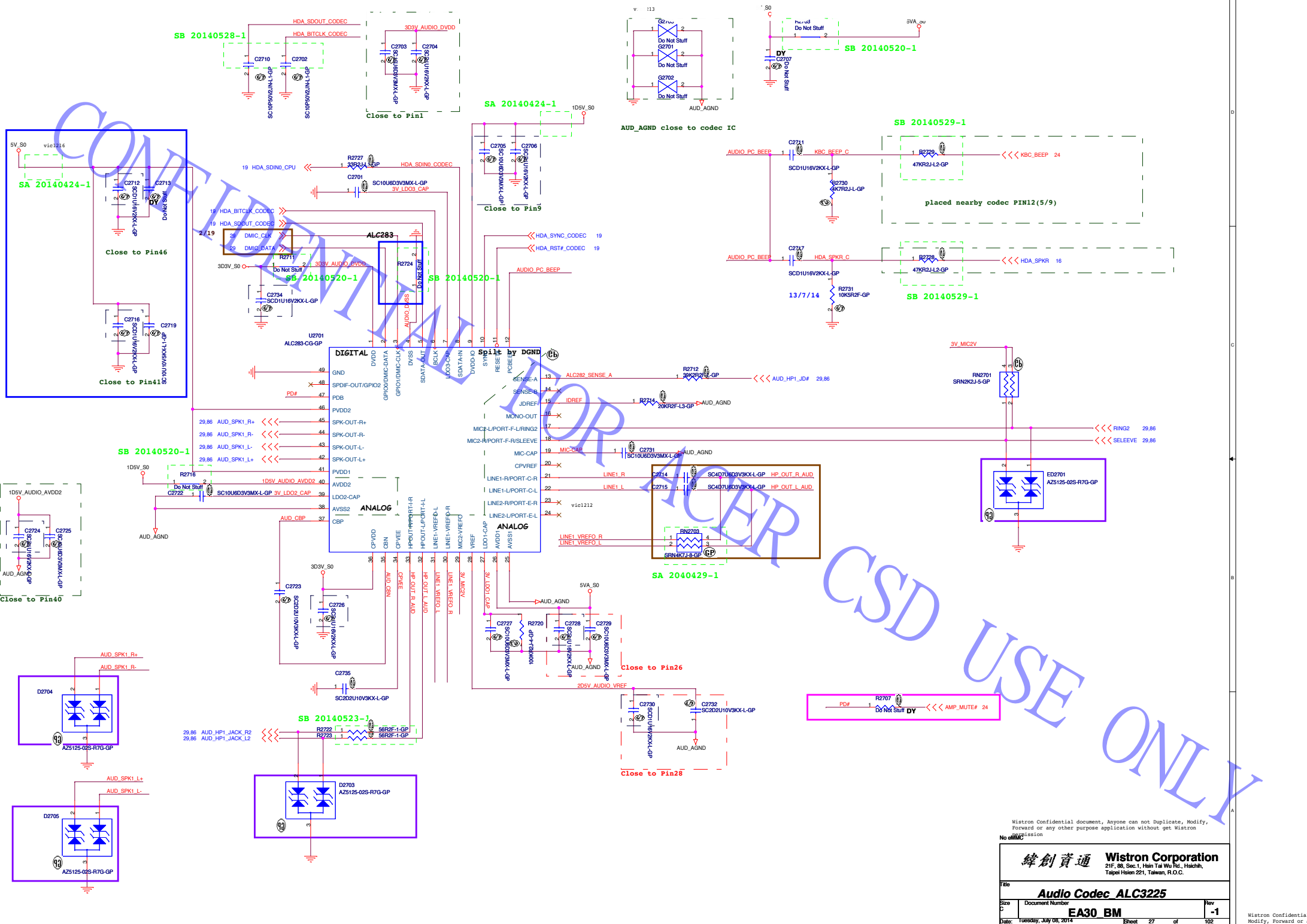
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
G788P81/Fan Controller P2793

Size A4 Document Number
EA30 BM

Date: Tuesday, July 08, 2014 Sheet 26 of 102

Rev
-1



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Title

Audio AMP 1001

Size

Document Number

Rev

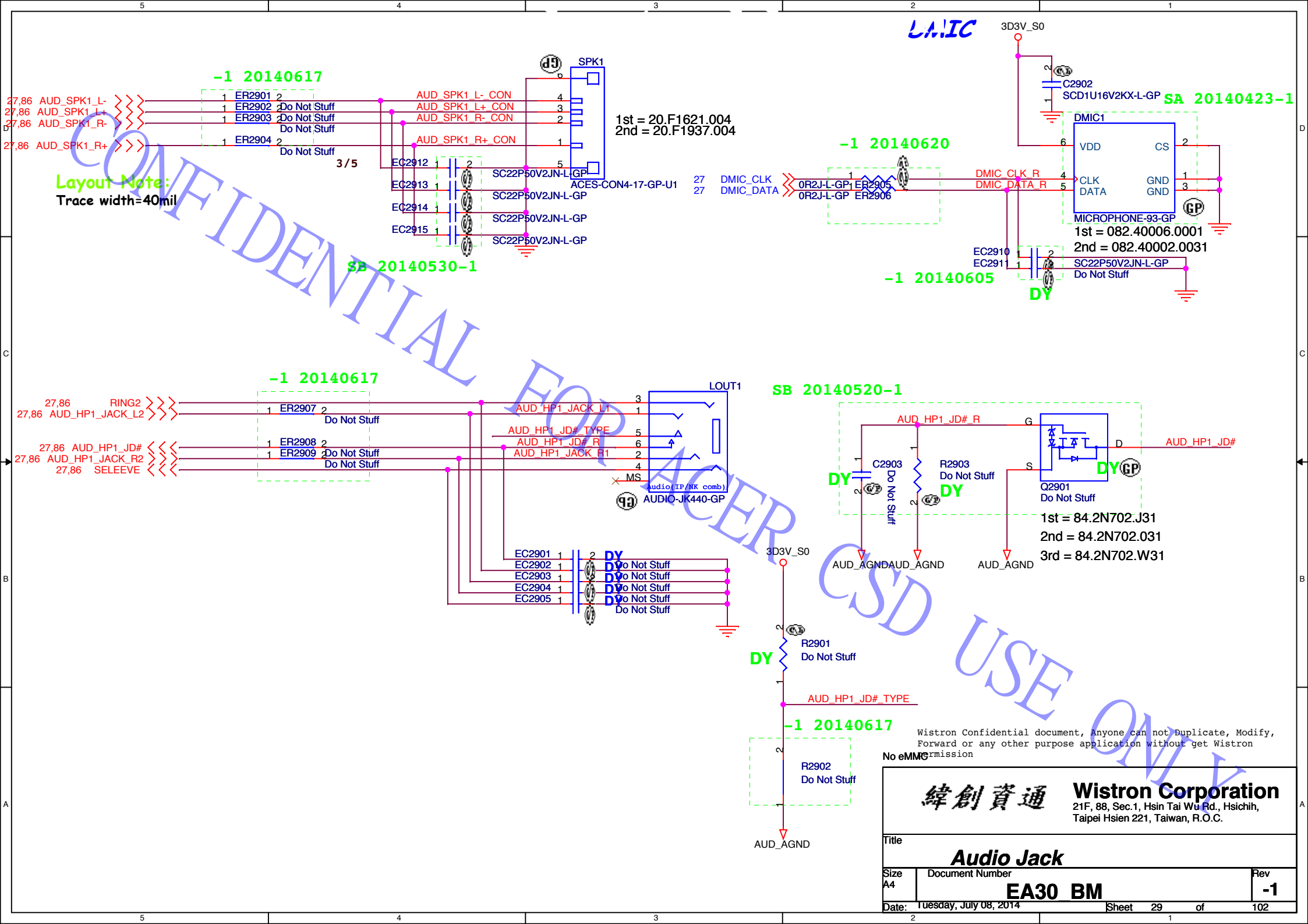
A4

EA30 BM

-1

Date: Tuesday, July 08, 2014

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Layout Note:
Trace width=40mil

1st = 20.F1621.004
2nd = 20.F1937.004

-1 20140620

SA 20140423-1

SB 20140530-1

-1 20140605

DY

-1 20140617

SB 20140520-1

DY

DY

DY

-1 20140617

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No eMMC

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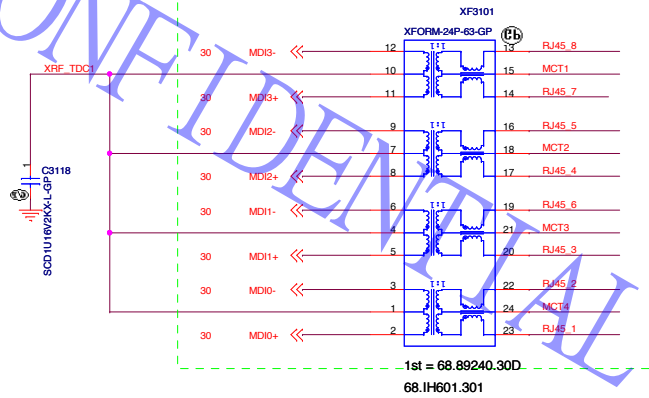
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Audio Jack		
Size	Document Number	Rev
A4	EA30 BM	-1
Date	Tuesday, July 08, 2014	Sheet 29 of 102

SSID = LAN

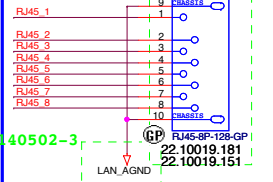
SB 20140528-1

RJ45_1 86
RJ45_2 86
RJ45_3 86
RJ45_4 86
RJ45_5 86
RJ45_6 86
RJ45_7 86
RJ45_8 86

SA 2040428-1



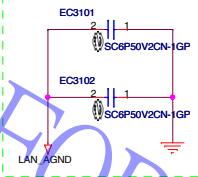
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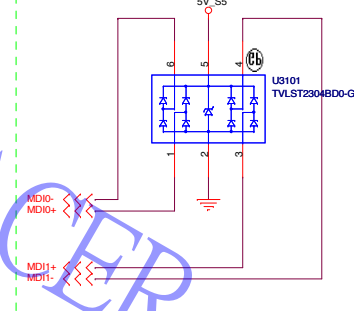
SA 20140502-3

LAN_RJ45 connector

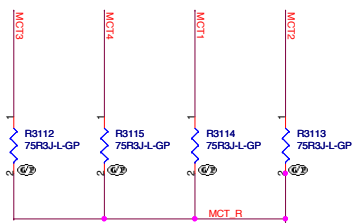
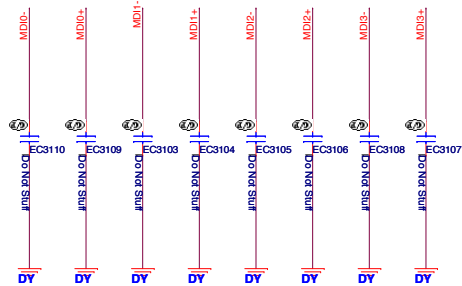
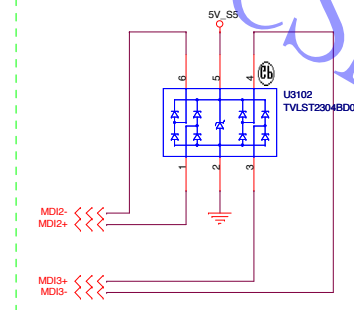
SA 20140506-2



SA 20140423-1



SA 20140423-1



SA 20140502-1

No eMMC

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Title

(LAN+VGA) CONNECTOR

Size

Document Number

EA30 BM

Rev

Date

1/8/2014, July 08, 2014

Sheet

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Title			
RTS5229(CARD READER)			
Size	Document Number		Rev
A4	EA30 BM		-1
Date: Tuesday, July 08, 2014		Sheet 32 of	102

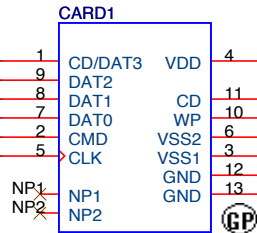
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SD//MS Card Reader

-1 20140605

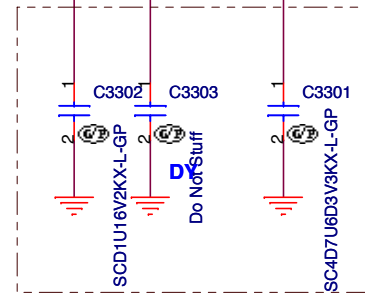
SA 20140505-1

30,86 SD_DATA3
30,86 SD_DATA2
30,86 SD_DATA1
30,86 SD_DATA0
30,86 SD_CMD
30,86 SD_CLK



Part Number = 62.10051.661
2nd = 62.10051.H51
3rd = 062.10002.0041

Close to Connector



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緯創資通		Wistron Corporation	
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Title			
CARD Reader CONN			
Size	Document Number	Rev	
Custom	EA30 BM	-1	
Date:	Tuesday, July 08, 2014	Sheet	33 of 102

USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

SB 20140522-1

2/19

SB 20140528-1

SB 20140521-1

SA 20140418

-1M 2040630

-1M 2040630

2nd = 83.3V3U4.0A0

1st = 22.10339.571

2nd = 69.10118.001
68.00396.001

SB 20140528-1

2nd = 69.10118.001
68.00396.001

-1M 2040630

-1M 2040630

SB 20140522-1

2/19

SB 20140521-1

No eMMC

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Taipei Hsien 221, Taiwan, R.O.C.

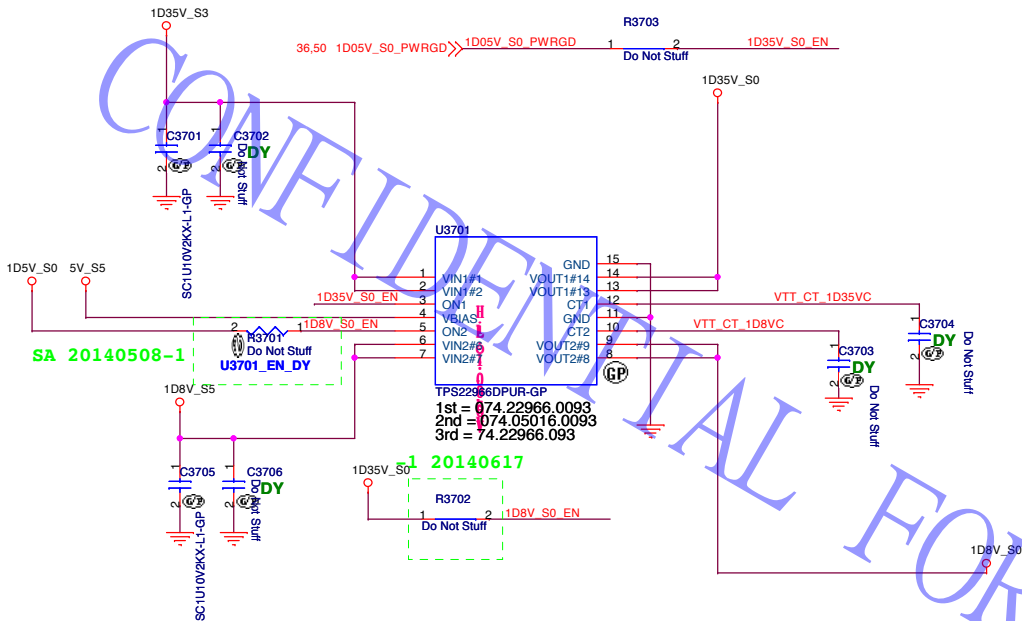
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Size A3	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 34 of 102	

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緯創資通		Wistron Corporation	
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Title			
USB CHARGER			
Size	Document Number		Rev
A3	EA30 BM		-1
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1D35V_S0
1D8V_S0



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Title ADAPTER OCP / S3 reduction		
Size A3	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014 Sheet 37 of 102		

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Title			
DS3			
Size	Document Number		Rev
A4	EA30 BM		-1
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Power Sequence

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Title

1D05 M

Size

Document Number

Rev

Custom

EA30 BM

-1

Date: Tuesday, July 08, 2014

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Title Connected Standby1			
Size A	Document Number EA30 BM		Rev -1
Date: Tuesday, July 08, 2014		Sheet 40 of	102

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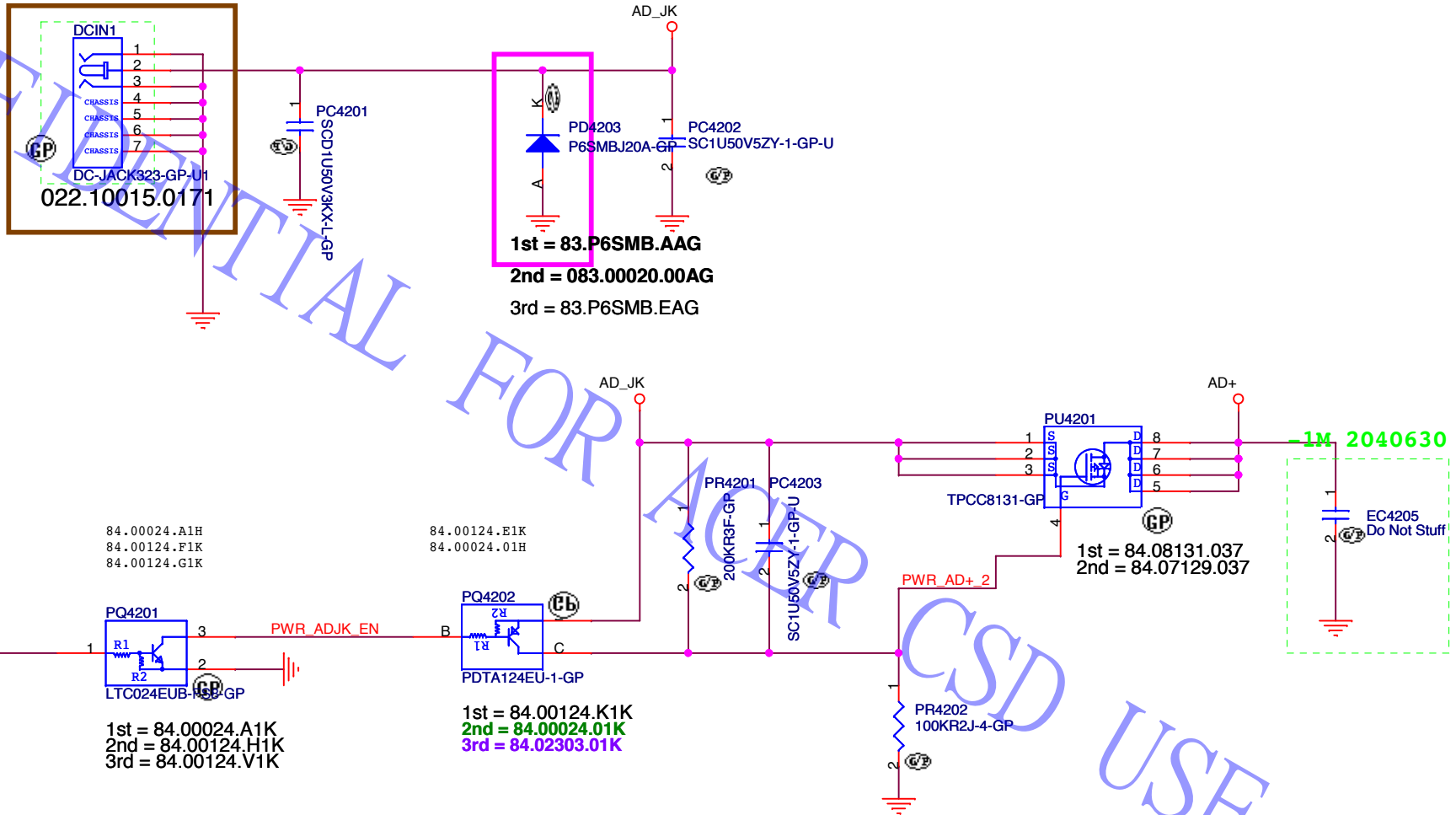
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Title			
Connected Standby2			
Size	Document Number		Rev
A	EA30 BM		-1
Date:	Tuesday, July 08, 2014		Sheet 41 of 102

ANNIE solution

Adaptor in to generate DCBATOUT

3/4 SA 20140418



vic0103



DC IN connector

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Title

DCIN JACK

Size
A4

Document Number

EA30 BM

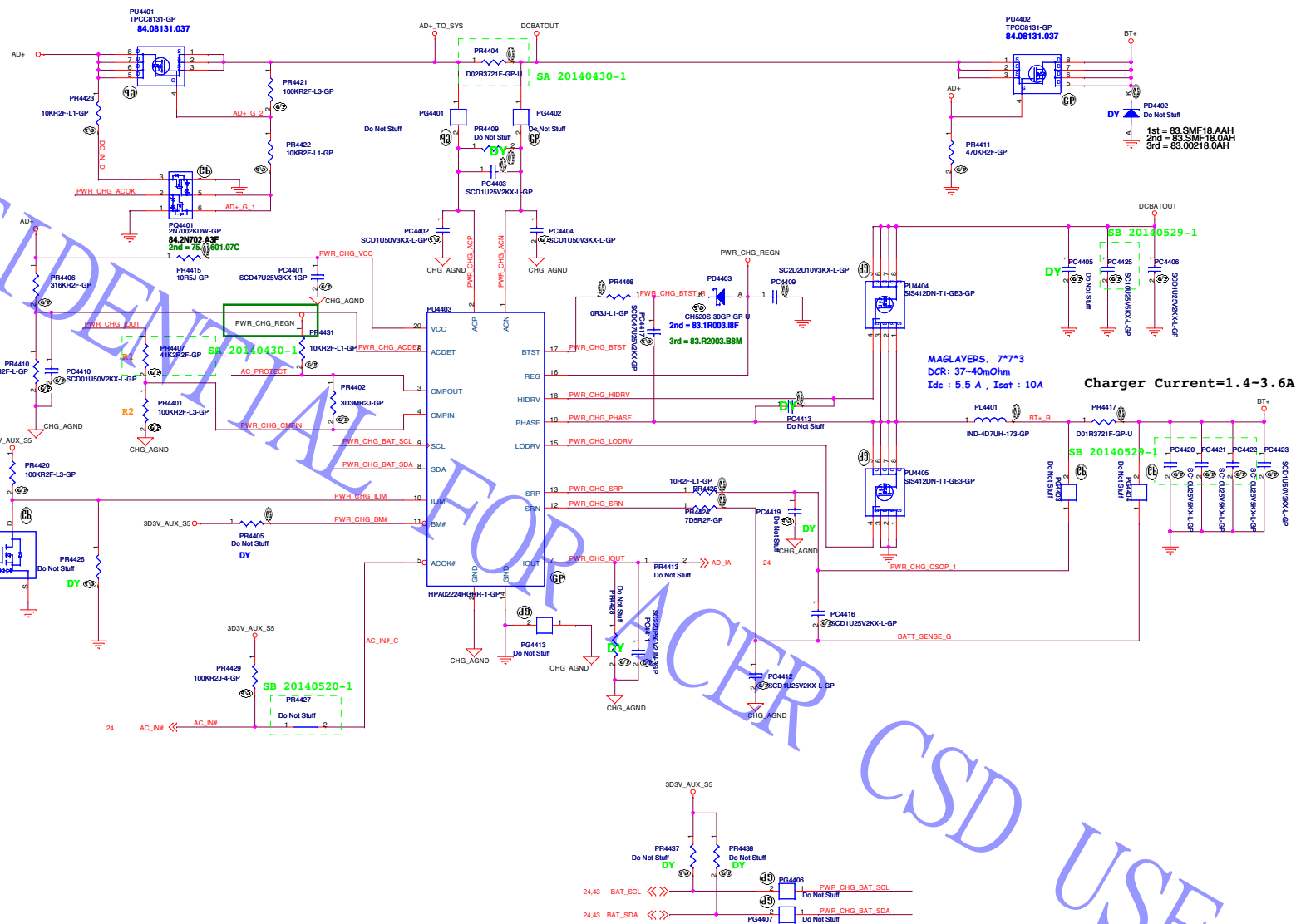
Rev
-1

Date: Tuesday, July 08, 2014

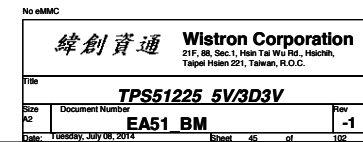
Sheet 42 of 102

SSID = Charger

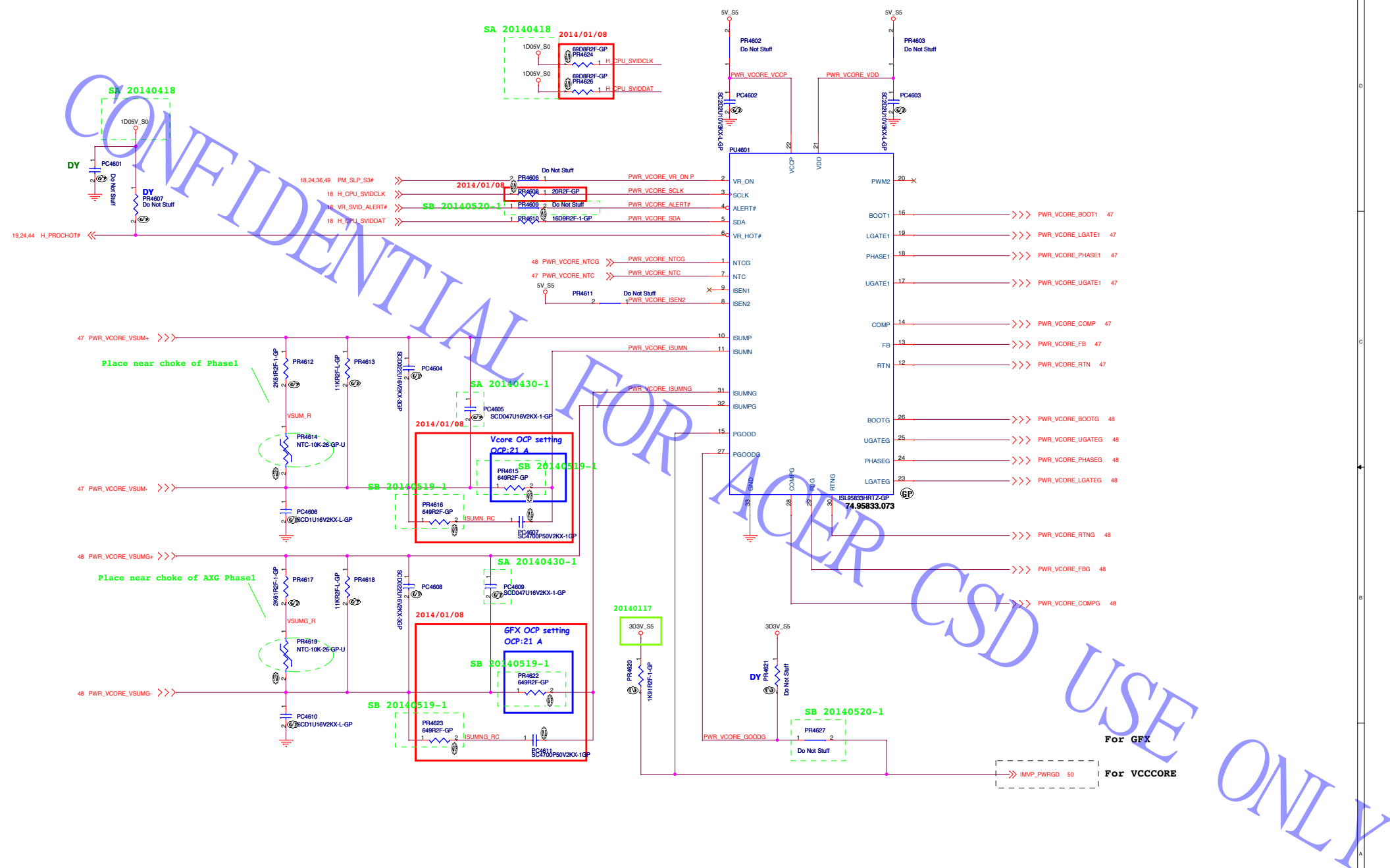
AD+ total power	R1	R2
40W	41.2K	100K

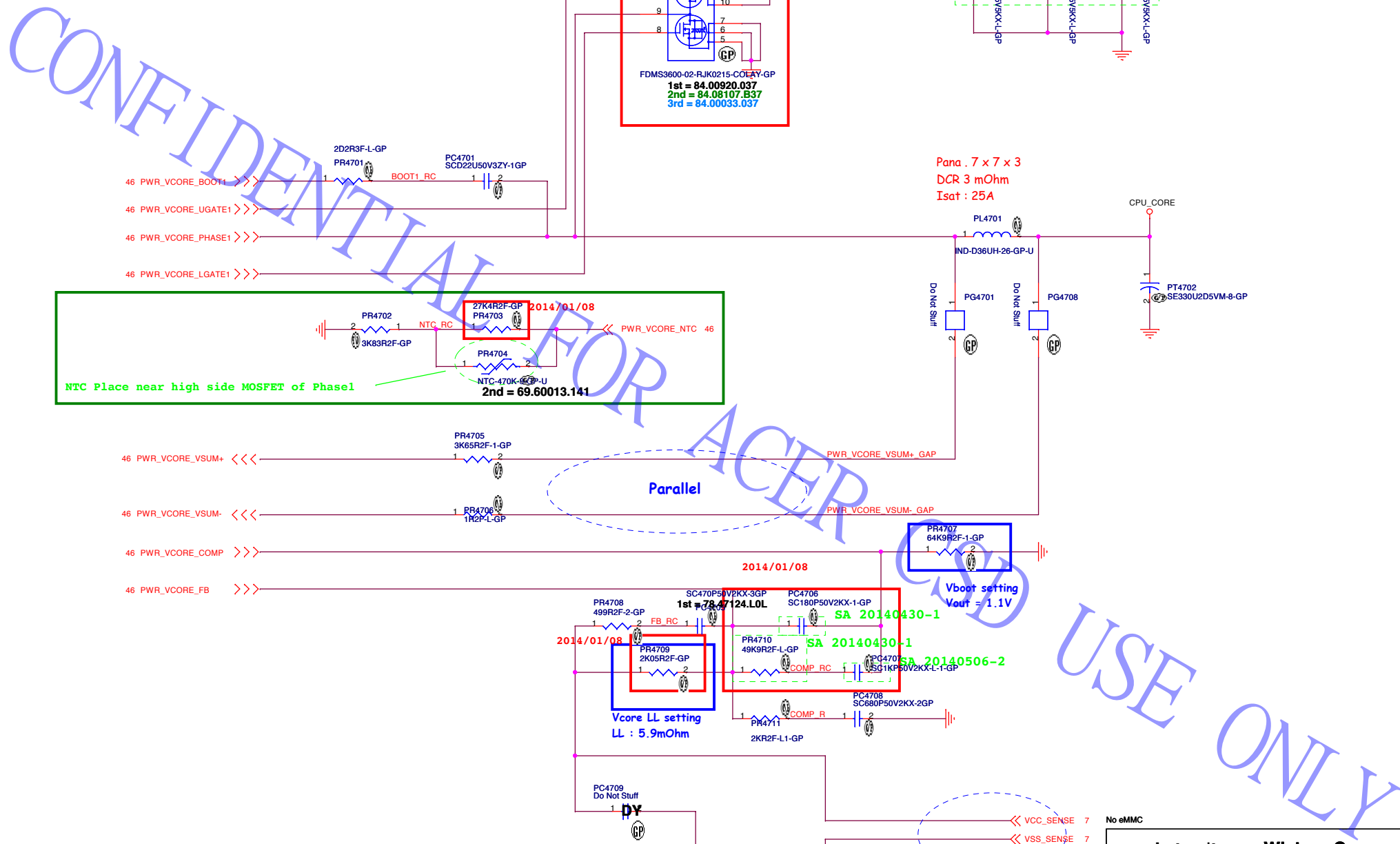


Title			
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Size A2	Document Number		Rev
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Date:	Tuesday, July 08, 2014	Sheet 44 of	102

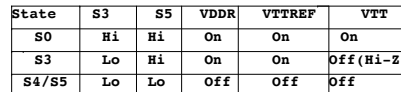


SSID = CPU.Regulator



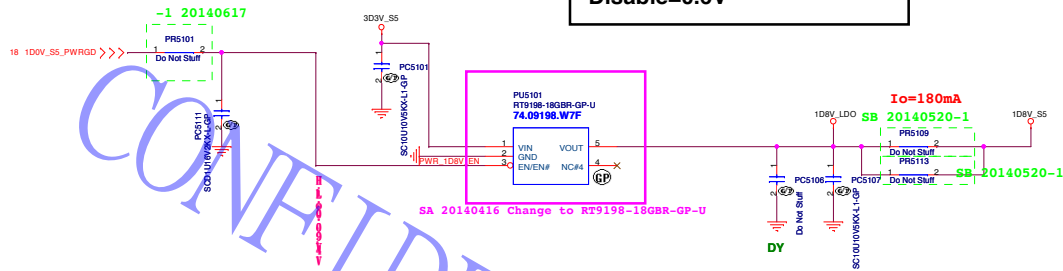


RT8231 for VDDQ



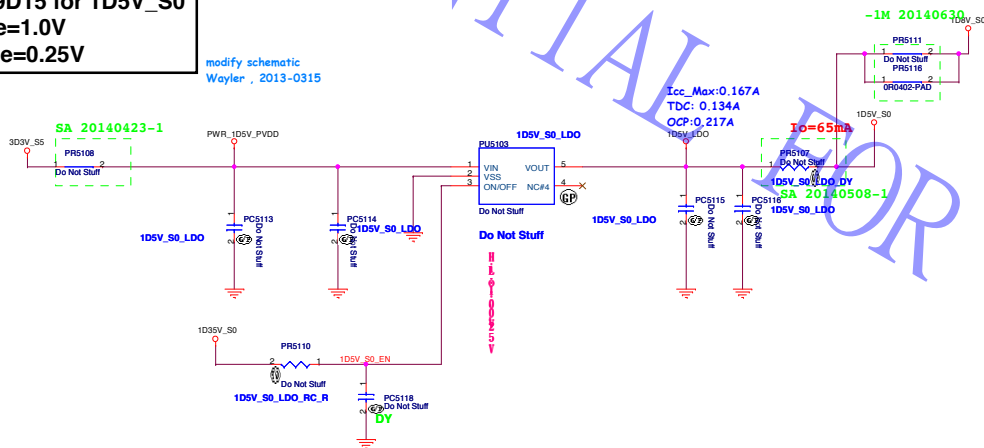
SSID = PWR.Plane.Regulator_1p8v

TLV70218DBVR for 1D8V_S1
Enable=0.9V
Disable=0.6V



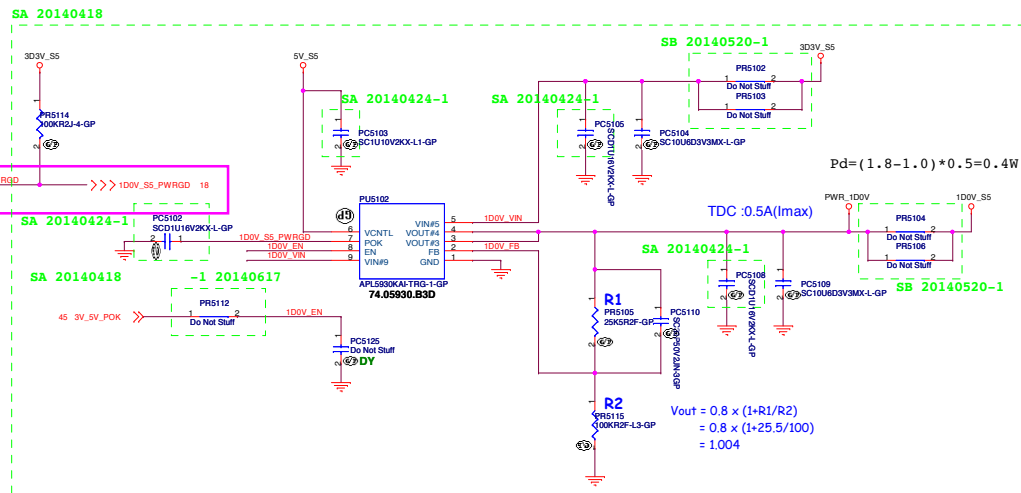
S-1339D15 for 1D5V_S0
Enable=1.0V
Disable=0.25V

modify schematic
Wayler, 2013-0315



20140418 Change to LDO

APL5930 for 1D0V_S5
Enable=1.1V
Disable=0.5V



No eMMC

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Title		LDO 1D8V&1D5V(SYW232)	
Size	Document Number	Rev	
A2	EA51 BM	-1	
Date: Tuesday, July 08, 2014		Sheet	61 of 102

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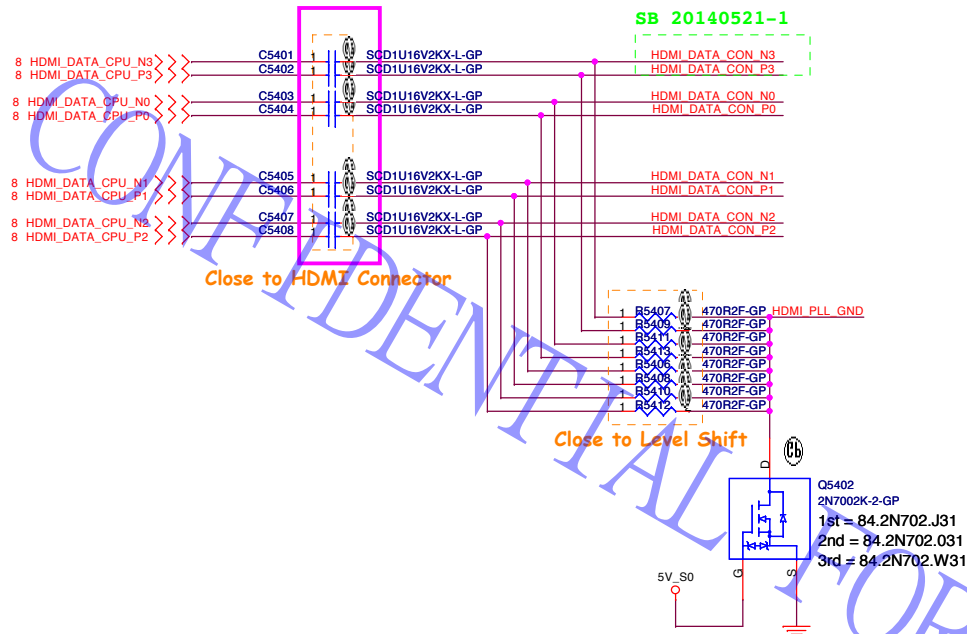
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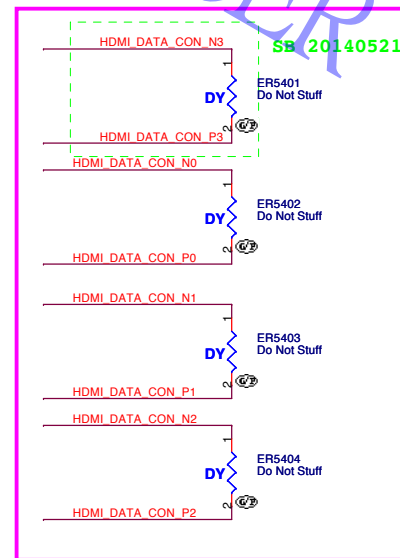
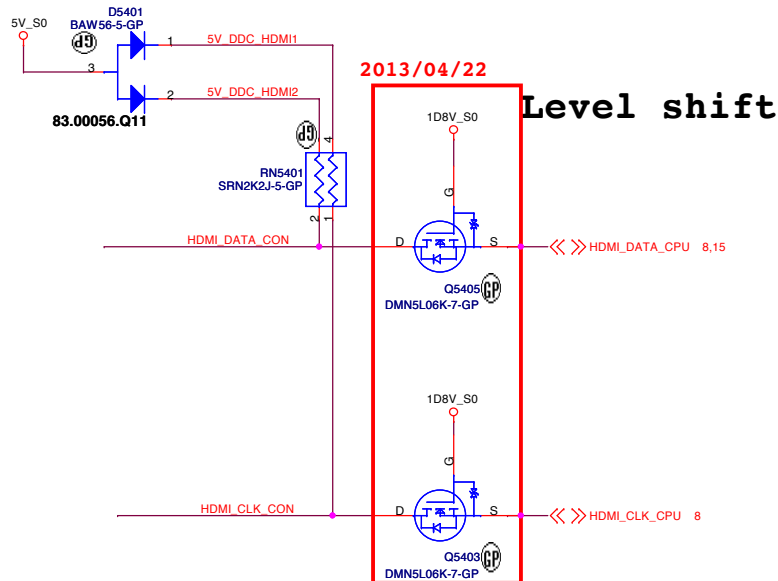
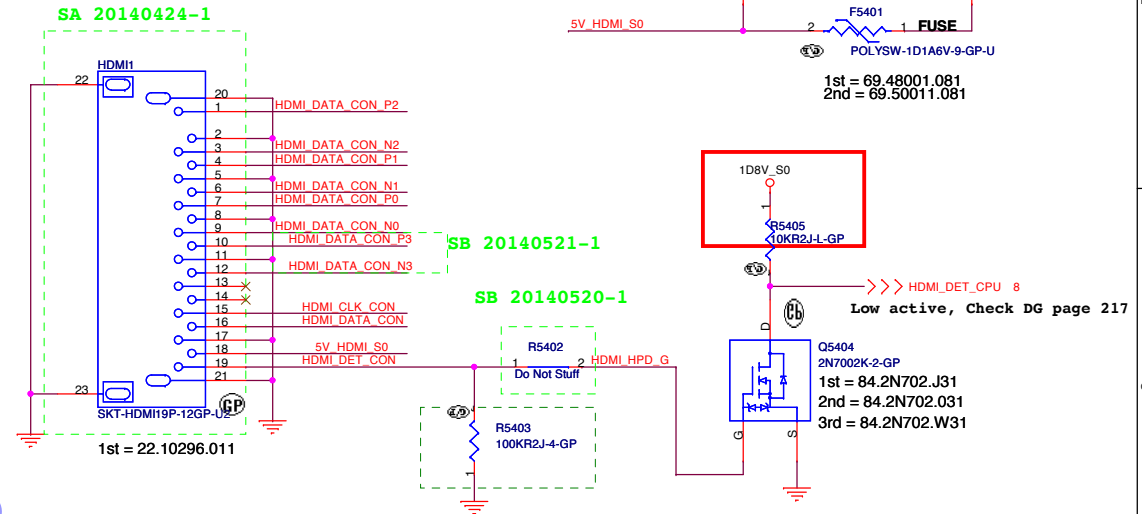
緯創資通		Wistron Corporation	
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Title			
CRT Board Connector			
Size	Document Number		Rev
A3	EA30 BM		-1
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SSID = VIDEO

HDMI Level Shifter & CONNECTOR



HDMI CONN



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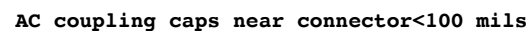
Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3	EA30 BM	-1
Date:	Tuesday, July 08, 2014	Sheet 54 of 102

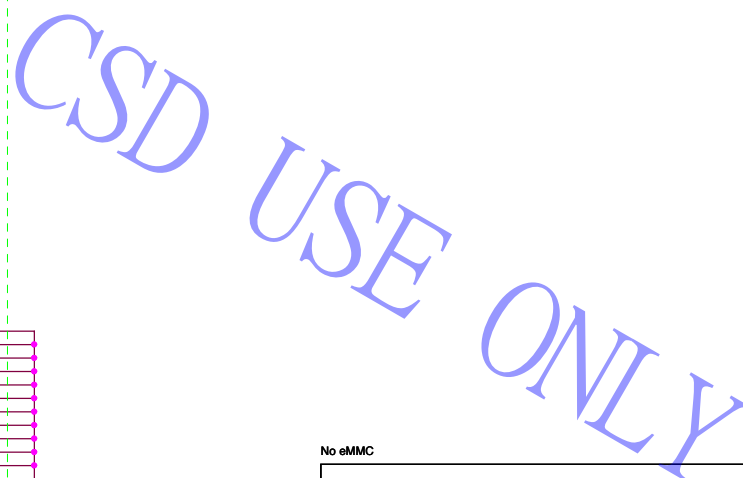
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<div>Title</div>					
<div>Display Port</div>					
<div>Size</div>	<div>Document Number</div>				<div>Rev</div>
<div>A3</div>	<div>EA30 BM</div>				<div>-1</div>
<div>Date:</div>	<div>Tuesday, July 08, 2014</div>			<div>Sheet</div>	<div>55 of 102</div>

SSID = SATA





SSID = Wireless *Mini Card Connector (602.11a/b/g/n)*



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Taipei Hsien 221, Taiwan, R.O.C.

MINICARD(WLAN)

Rev

1107

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SSID = Wireless

Mini Card Connector(mSATA)

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Title			
WWAN CONN			
Size	Document Number		Rev
A4	EA30 BM		-1
Date: Tuesday, July 08, 2014		Sheet 59	of 102

SSID = mSATA

Mini Card Connector(mSATA)

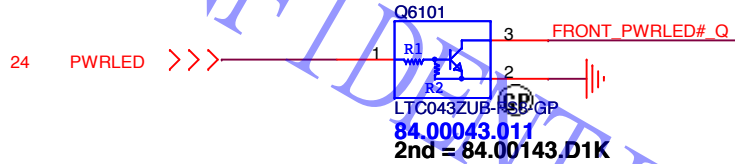
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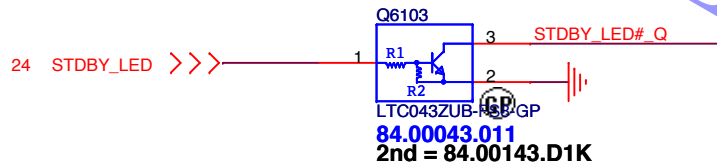
No eMMC

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
mSATA Connector			
Size	Document Number		Rev
A4	EA30 BM		-1
Date: Tuesday, July 08, 2014		Sheet 60 of	102

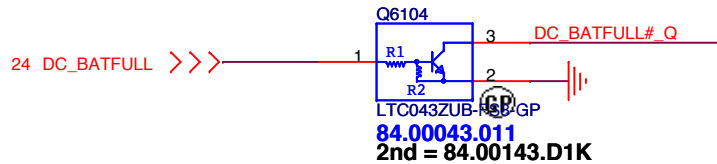
Power button_LED



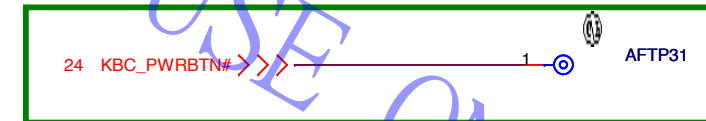
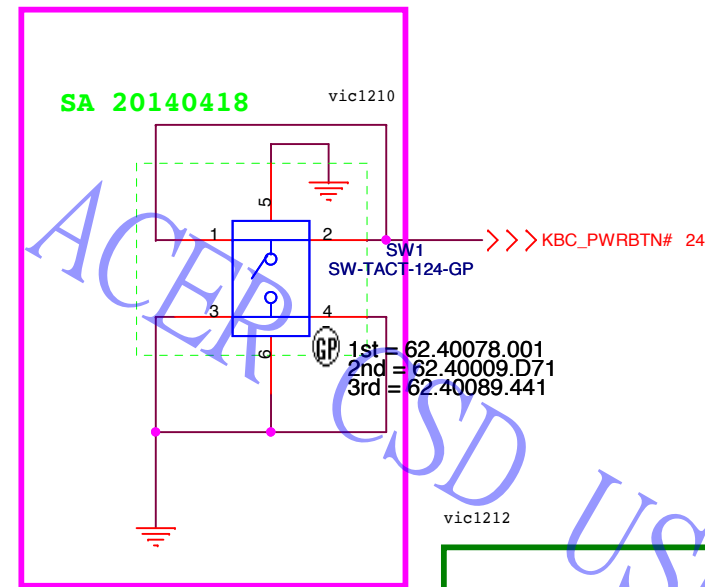
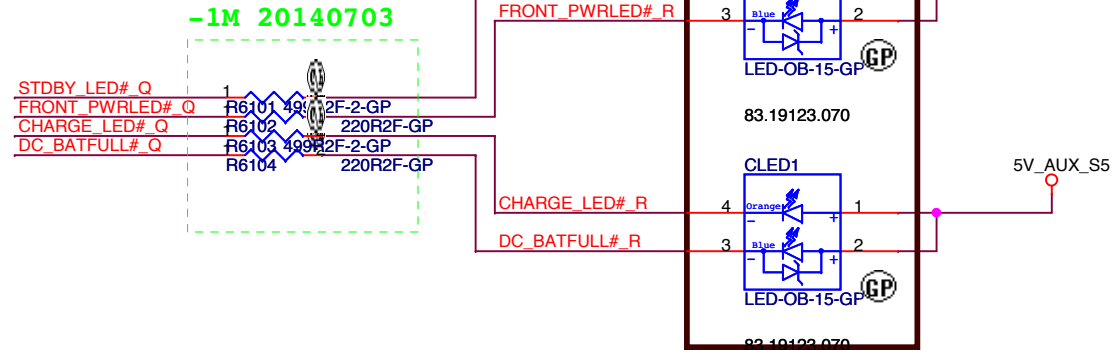
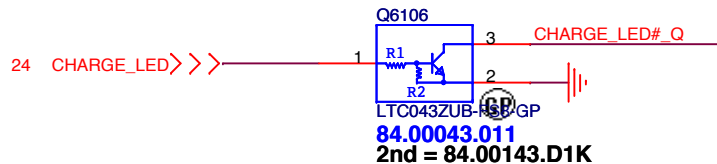
Power STDBY_LED



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)

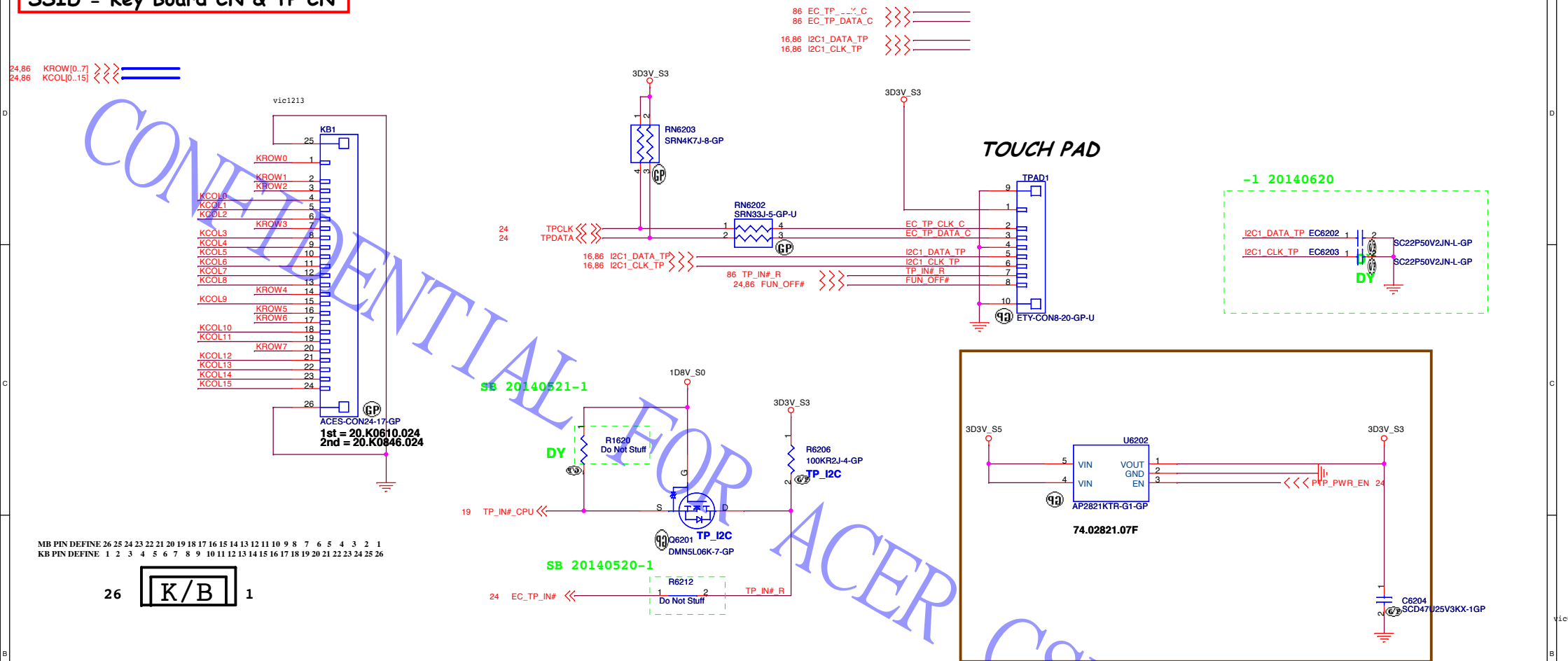


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Title		
LED Bard/Power Button		
Size	Document Number	Rev
A4	EA30 BM	-1
Date:	Tuesday, July 08, 2014	Sheet 61 of 102

SSID = Key Board CN & TP CN



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Title

Key Board/Touch Pad

Size

Document Number	
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EA30_BM

Rev

1.

Date: Tuesday, July 08, 2014

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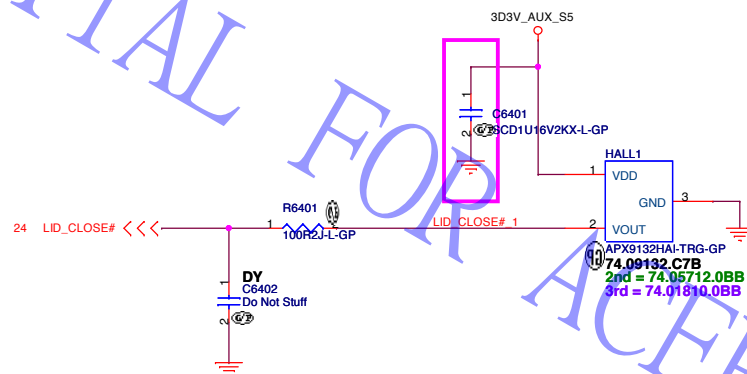
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Title			
IO Board Connector			
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size

Document Number

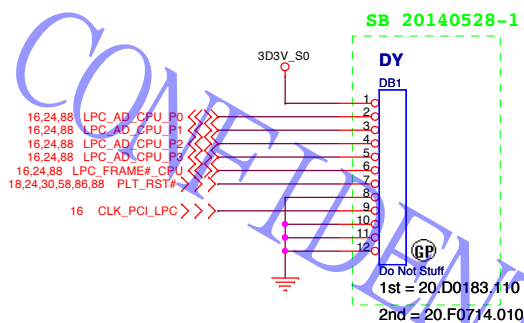
EA30 BM

Rev

-1

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Title			
SENSOR HUB			
Size	Document Number		Rev
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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Title

G Sensor

Size
A

Document Number

EA30 BM

Rev

-1

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Title			
Thunderbolt (1/5)			
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Date:	Tuesday, July 08, 2014	Sheet 68	of 102

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Title			
Thunderbolt (2/5)			
Size	Document Number		Rev
Custom	EA30 BM		-1
Date:	Tuesday, July 08, 2014	Sheet 69 of	102

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Title			
Thunderbolt (3/5)			
Size	Document Number		Rev
Custom	EA30 BM		-1
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Title	
Thunderbolt (4/5)	
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-1	

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Title			
Thunderbolt (5/5)			
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Title GPU(PEG)			
Size	Document Number	Rev	
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Title			
GPU (DIGITALOUT)			
Size	Document Number		Rev
Custom	EA30 BM		-1
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<div>緯創資通 Wistron Corporation</div> <div>21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title GPU (VRAM VF)		
Size A2	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014 Sheet 75 of 102		

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No 6686C	
緯創資通 Wistron Corporation 21F, No. 306, L. 10th St. Taipei, Taiwan, R.O.C.	
GPU (GPIO/STRAP)	
Doc	Rev
EA30 BM	-1

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Title GPU (POWER/GND)			
Size	Document Number	Rev	
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Title			
GPU-VRAM1,2 (1/4)			
Size	Document Number		Rev
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Title			
GPU-VRAM3,4 (2/4)			
Size	Document Number	Rev	
Custom	EA30 BM	-1	
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Title			
GPU-VRAM5,6 (3/4)			
Size	Document Number	Rev	
Custom	EA30 BM	-1	
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Title			
GPU-VRAM7,8 (4/4)			
Size	Document Number		Rev
Custom	EA30 BM		-1
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Title			
RT8812A VGA CORE			
Size	Document Number		Rev
Custom	EA30 BM		-1
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DISCRETE VGA POWER					
Doc		Document Number		Rev	
Date		EA30 BM		-1	
CSD		URGENCY: DAYTIME		Page 83 of 88	

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Title			
Switchable GFX LCD(1/2)			
Size	Document Number		Rev
A4	EA30 BM		-1
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Title			
Switchable GFX LCD(2/2)			
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SA 20140430-1

SA 20140422-1

H3 Do Not Stuff

SA 20140506-1

SB 20140528-1

01 04 2 1

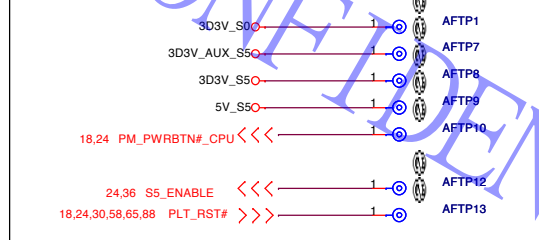
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SA 20140430-1

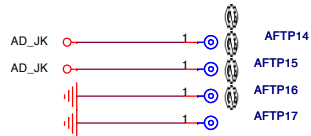
SB 20140521-1

Check test point

Test Point放在 Bottom side 可量測處

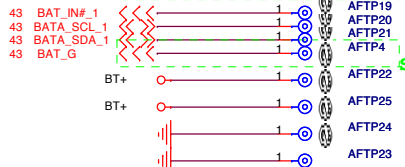


DCIN

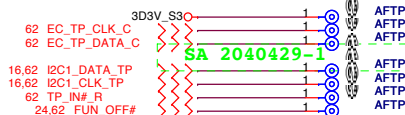


BARRETY

SA 2040429-1



Touch PAD



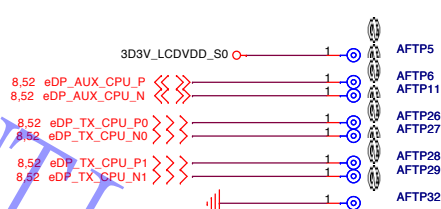
Speaker



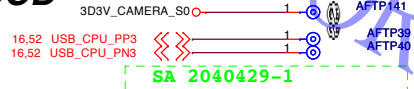
DMIC

SA 2040429-1

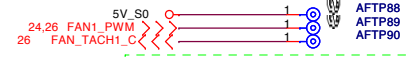
eDP



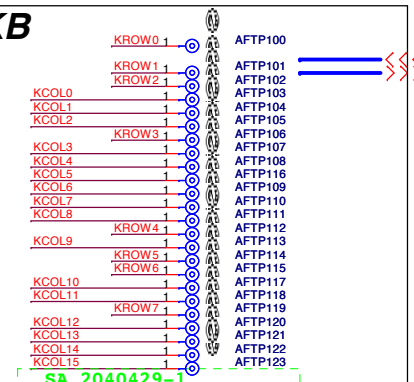
CCD



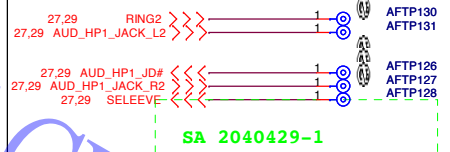
FAN



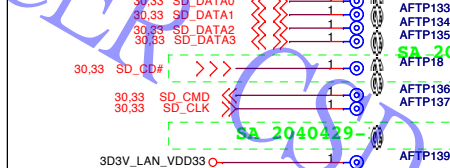
KB



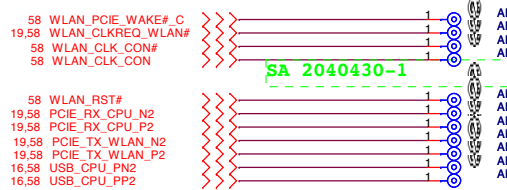
Audio Jack



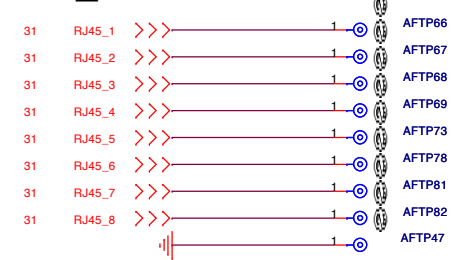
Card reader



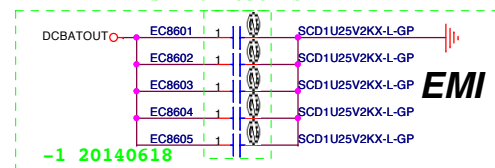
WLAN



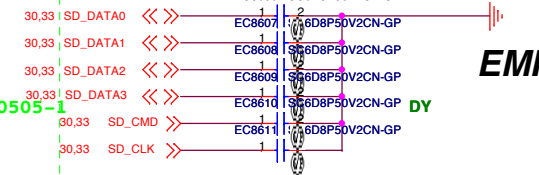
LAN_RJ45 connector



SA 20140502-3

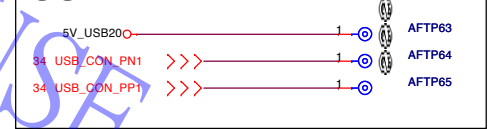


-1 20140618



USB2

SB 20140528-1



No eMMC

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Taipei Hsien 221, Taiwan, R.O.C.

Title

UNUSED PARTS/EMI Capacitors

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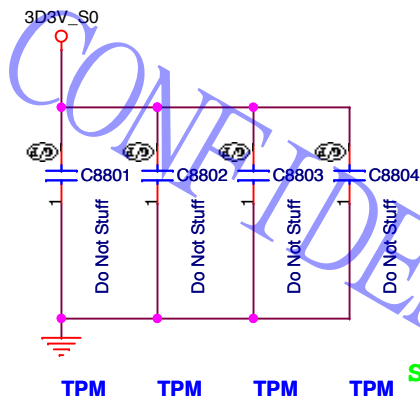
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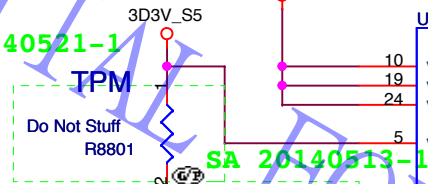
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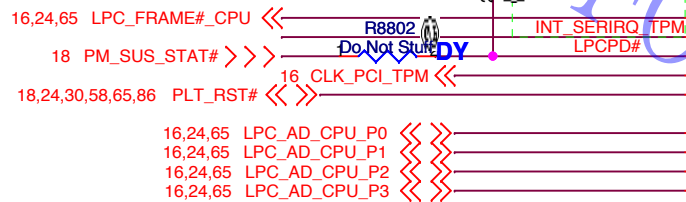
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SB 20140521-1

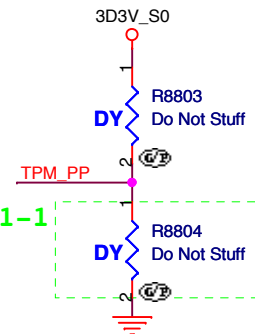


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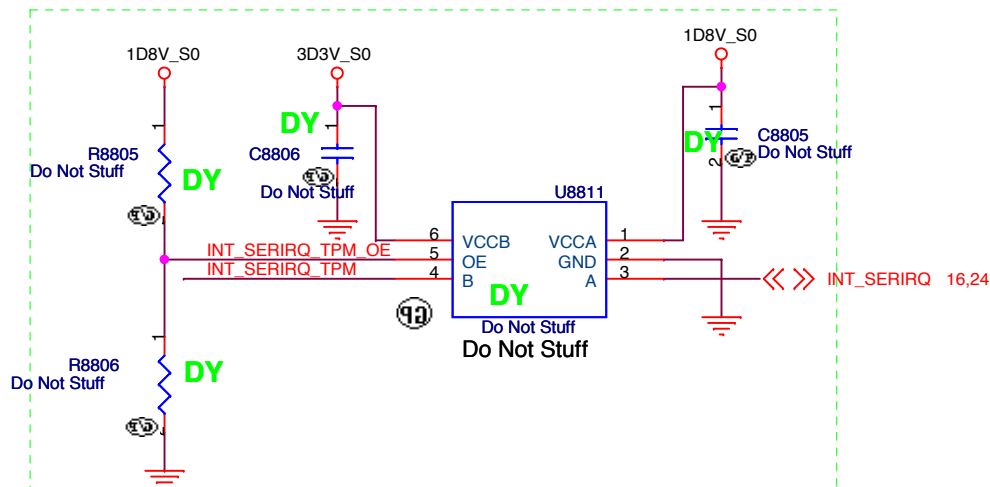


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SB 20140521-1



SB 20140513-1



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Title Smart Card socket			
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Title Switchable GFX eDP			
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Title Bottom Docking			
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Title		
Inter LAN WG1217LM		
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Title			
LAN Switch			
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title PCH_XDP			
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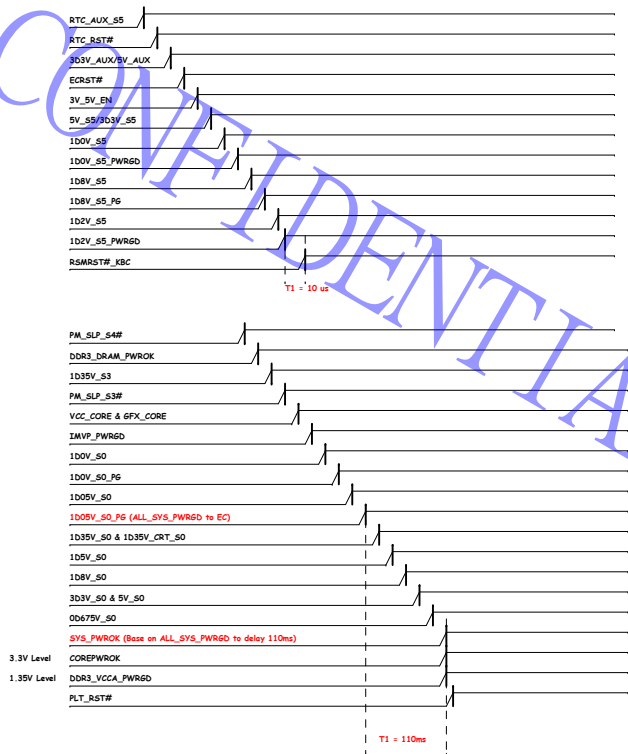
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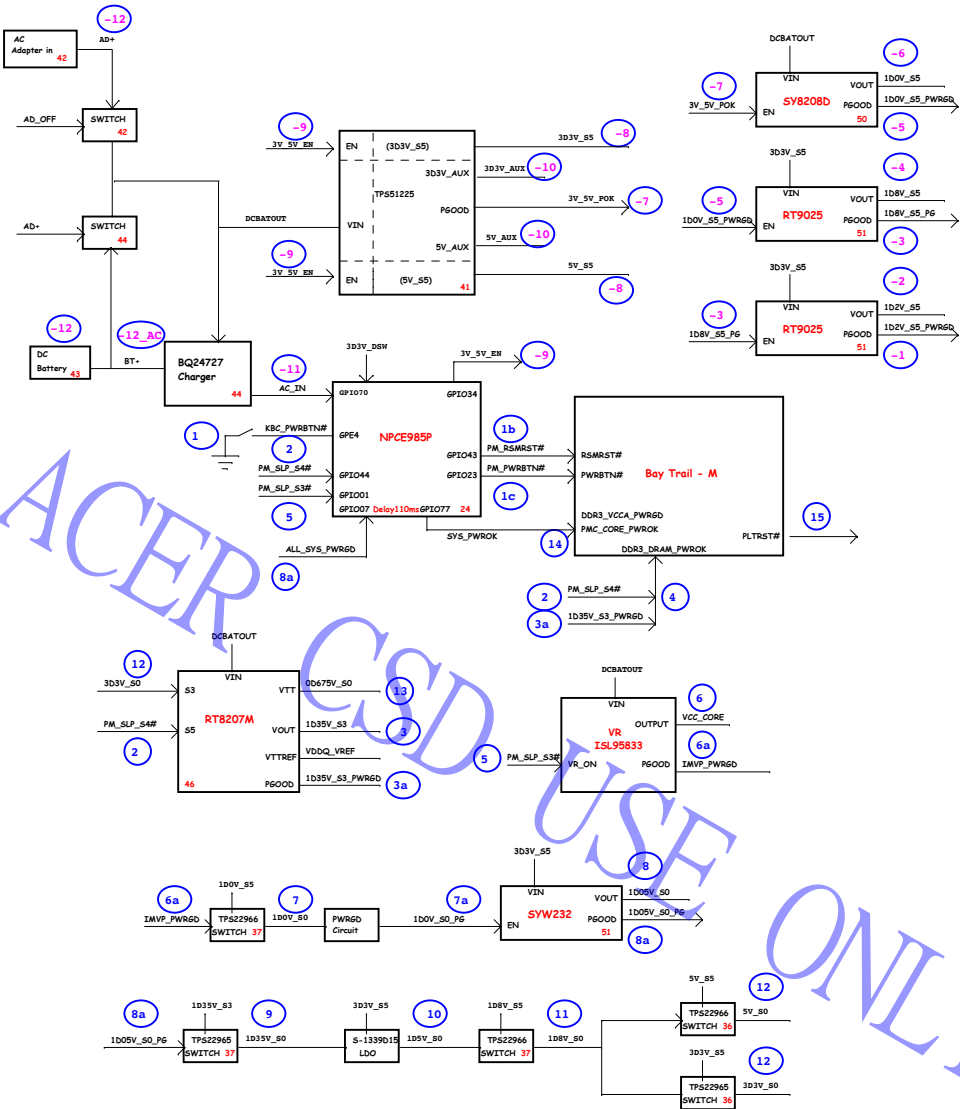
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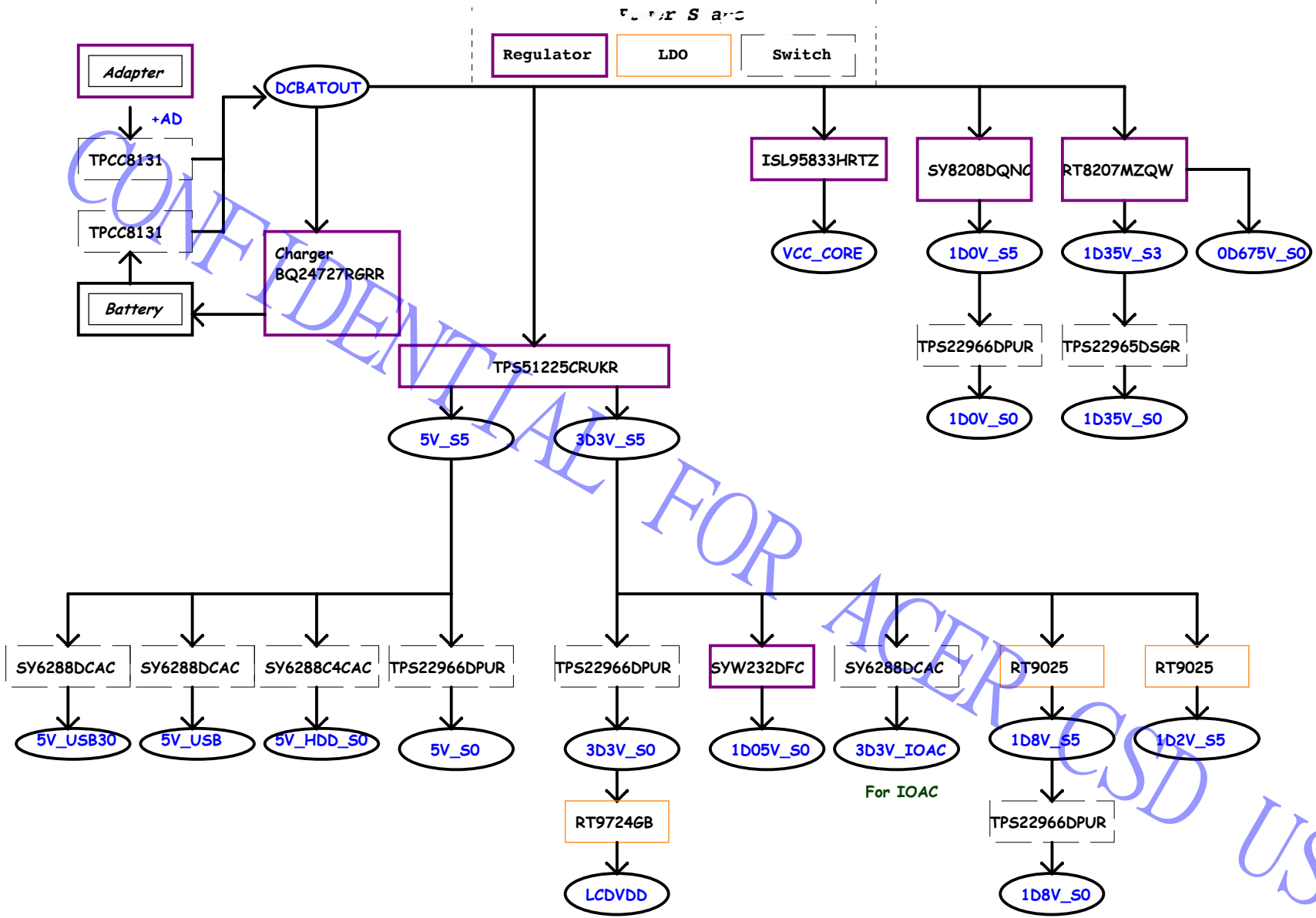
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Intel-Power Up Sequence with non-S0ix



Bay Trail - M POWER UP SEQUENCE DIAGRAM

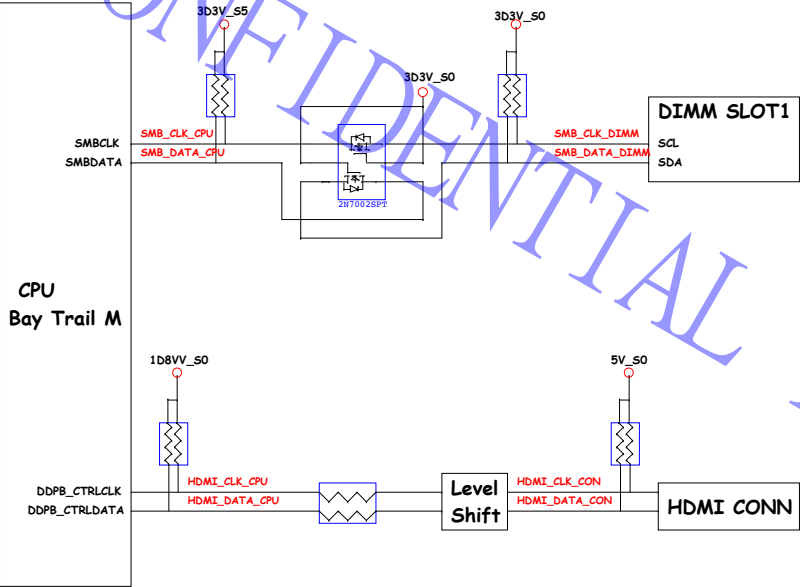




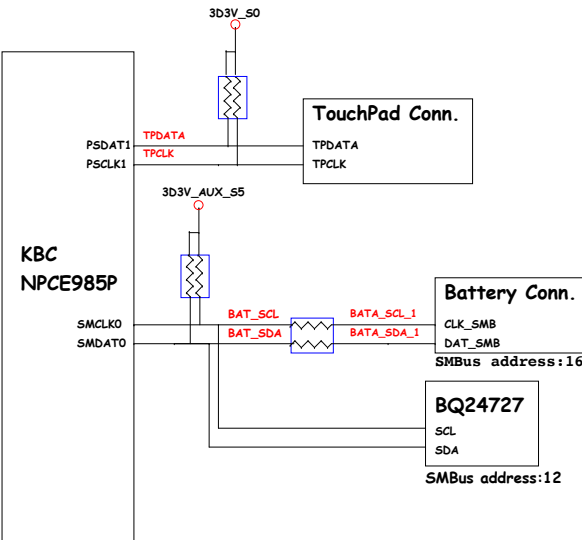
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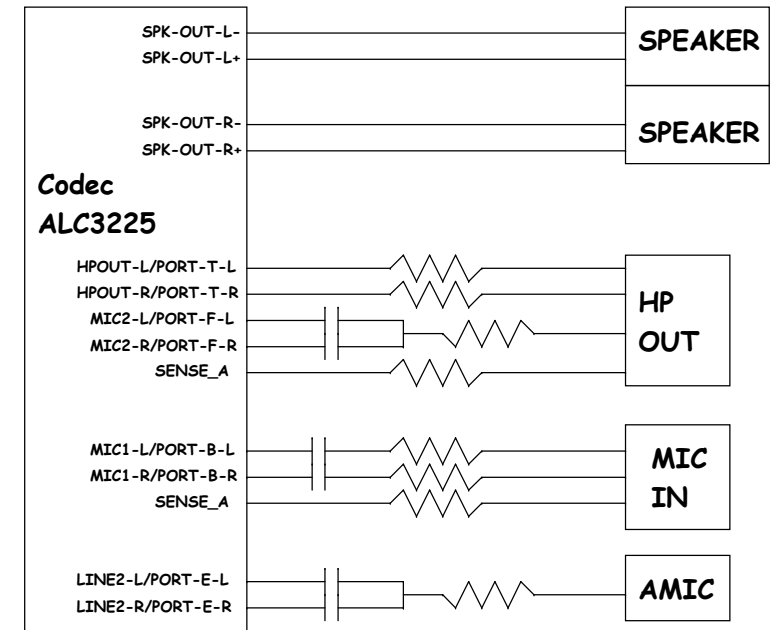
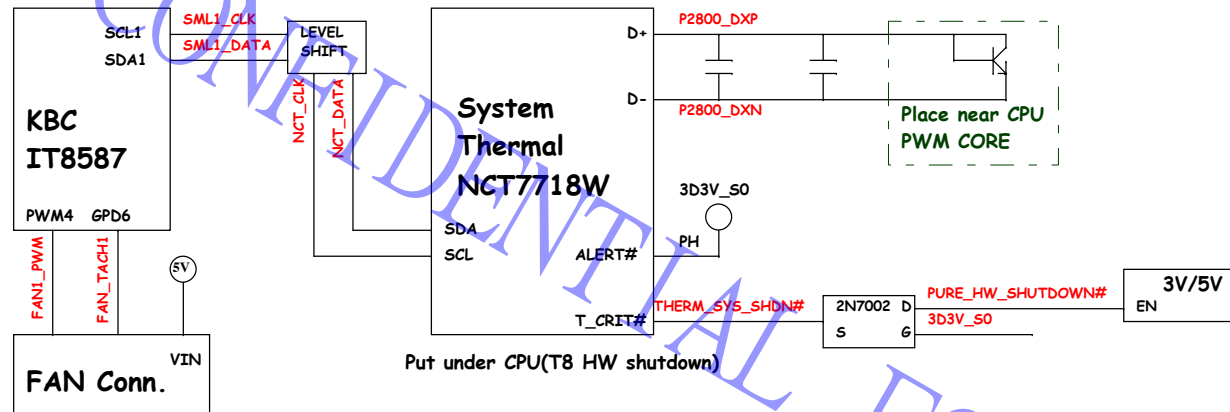
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Audio Block Diagram



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